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Synaptic devices based on purely electronic memristors

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Memristive devices have been widely employed to emulate biological synaptic behavior. In these cases, the memristive switching generally originates from electrical field induced ion migration or Joule heating induced phase change. In this letter, the Ti/ZnO/Pt structure was found to show memristive switching ascribed to a carrier trapping/detrapping of the trap sites (e.g., oxygen vacancies or zinc interstitials) in ZnO. The carrier trapping/detrapping level can be controllably adjusted by regulating the current compliance level or voltage amplitude. Multi-level conductance states can, therefore, be realized in such memristive device. The spike-timing-dependent plasticity, an important Hebbian learning rule, has been implemented in this type of synaptic device. Compared with filamentary-type memristive devices, purely electronic memristors have potential to reduce their energy consumption and work more stably and reliably, since no structural distortion occurs. © *2016 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4939436]

Synaptic electronics aims to build artificial devices that demonstrate behavior similar to synapses in the biological nervous system.[1,2] Synaptic device is the most important component of next-generation neuromorphic computers allowing a new and more powerful approach to computing.[3,4] Memristors, exhibiting a distinctive "fingerprint" characterized by a pinched hysteresis loop confined to the first and the third quadrants of the *I–V* plane,[5] are ideal for synaptic device applications due to their superior performance such as high scalability, low power consumption, and controllable multilevel resistance states.[6] Memristive devices based on non-volatile resistive switching have been employed to emulate synaptic behavior, in which various switching media were used such as oxides,[7–12] chalcogenides,[13–17] silicon,[18] carbon,[19] and polymers.[20,21] In these cases, the memristive switching generally originates from electrical field induced ion migration or Joule heating induced phase change.[7–11,14–21]

ZnO-based memristive devices using metals (Cu, Ag, Pt, etc.),[22–26] conducting oxides (In_2O_3:Sn, ZnO:Al, etc.),[27,28] or conducting nitrides (TiN, etc.) (Ref. 29) as electrodes have been widely investigated. In all such devices, the formation/rupture of conducting filaments accounts for the resistive switching. In this study, Ti was employed as the top electrode and Pt as the bottom electrode. The Ti/ZnO/Pt structure shows memristive switching ascribed to a carrier trapping/detrapping of the trap sites (e.g., oxygen vacancies V_O or zinc interstitials Zn_i) in ZnO. Continuous RESET (ON-to-OFF switching) and SET (OFF-to-ON switching) processes have been realized in such purely electronic memristive device. Furthermore, spike-timing-dependent plasticity (STDP) learning rule has been implemented in this type of synaptic device.

Polycrystalline ZnO films with a thickness of ~100 nm were deposited on Pt/Ti/SiO_2/Si substrates at room temperature (RT) by RF magnetron sputtering of a ZnO target under Ar/O_2 ambient.[23,24,30] 50 nm thick Ti top electrodes with a diameter of 200 μm were deposited on ZnO films at RT by electron-beam evaporation with an *in situ* metal shadow mask. To prevent Ti from oxidizing, a 20 nm thick Au protection layer was deposited on the Ti electrodes by electron-beam evaporation. The Ti/ZnO/Pt devices were then annealed at 100 °C under Ar ambient for 10 min. Electrical characteristics of Ti/ZnO/Pt were measured at RT in air using a Keithley 4200 semiconductor parameter analyzer. During the measurement in voltage sweeping (DC) and pulse modes, the bias voltage was applied to the top electrode (Ti) while the bottom electrode (Pt) was grounded. The voltage sweeping rate was set to be 0.35 V/s. For conducting atomic force microscopy (CAFM) measurement, 150 nm thick Ti top electrodes with a diameter of 40 μm were employed, while keeping other preparation conditions unchanged. Before the CAFM measurement, the devices underwent an electroforming process followed by removing the Ti electrodes using an adhesive tape.

Figure 1(a) presents the *I–V* characteristics of Ti/ZnO/Pt showing a typical non-volatile bipolar memristive switching performance. The inset shows the corresponding *I–V* curves in semilogarithmic scale. The figure displays the electroforming process (switching from the initial state to an ON state) and subsequent RESET and SET processes. During electroforming and SET, a current compliance (CC) was employed to control current flowing through the device. The important feature of Fig. 1(a) is the nonlinear *I–V* characteristics in ON state of the memristive device. Figure 2(a) shows resistance versus temperature plots for Ti/ZnO/Pt in ON and OFF states. Both states exhibit a typical semiconducting behavior, since the resistance decreases strongly with temperature. Thus, two filamentary switching mechanisms can be excluded: (i) formation/rupture of complete conducting filaments in which the ON state resistance should

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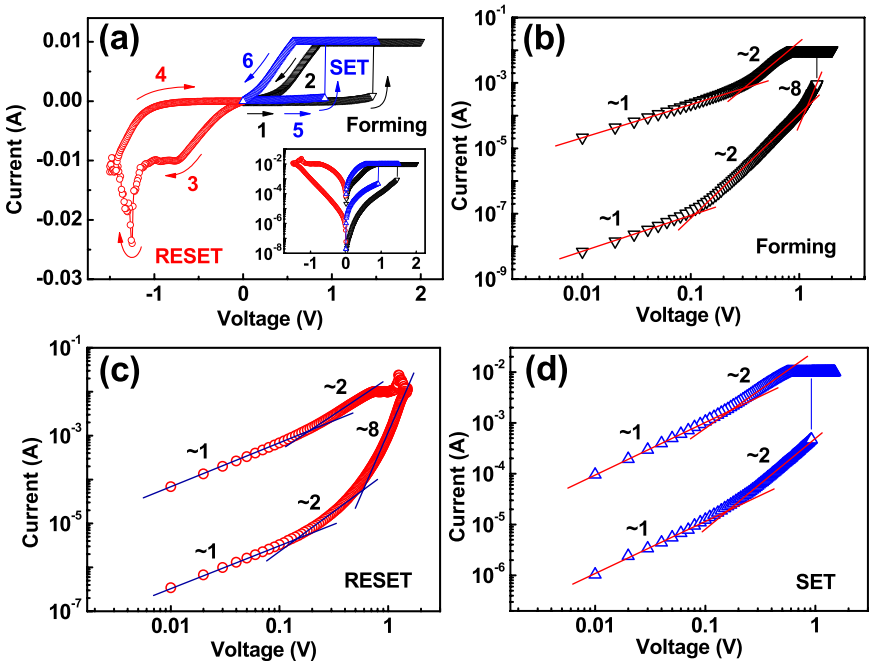

FIG. 1. (a) Typical *I*–*V* characteristics of the Ti/ZnO/Pt structure. The inset shows the *I*–*V* curves in semilogarithmic scale. (b)–(d) *I*–*V* curves of the electroforming, RESET, and SET processes replotted in double-logarithmic scale and the linear fitting results. The corresponding slopes for different portions are also shown.

exhibit a typical metallic behavior, i.e., the resistance increases linearly with temperature, and (ii) formation/rupture of incomplete conducting filaments in which the ON state resistance should exhibit a typical tunneling behavior, i.e., the resistance decreases weakly with temperature.[19,31] Nonfilamentary switching mechanism in Ti/ZnO/Pt was further confirmed by a strong device size dependence of the resistance in both ON and OFF states, as shown in Fig. 2(b). The resistance decreases strongly with device size demonstrating that the current in both ON and OFF states should be dominated by a bulk conduction mechanism. (As for filamentary mechanisms, the ON state resistance is not dependent on device size.)[32] A still further confirmation of the nonfilamentary switching mechanism was obtained by cutting the top electrode of a device in ON or OFF state into two equal halves followed by comparing the resistance of the previous device and subsequent two halves. Forty devices were used to conduct such experiment, with 20 in OFF states and 20 in ON states. Figure 2(c) shows a comparison of the resistance of the previous whole devices (R_W) and subsequent half devices (R_H). Obviously, the R_H/R_W ratio of most devices in ON or OFF state is about two, confirming the bulk conduction mechanism for both ON and OFF states. Direct evidence for the bulk resistive switching mechanism for Ti/ZnO/Pt was provided by CAFM measurement, as shown in Fig. 2(d). The left and right panels are for the pristine and electroformed devices, respectively. Before the measurement, the Ti top electrodes were removed by adhesive tape. We can see that at 2 V read voltage, no obvious current is observed for the pristine device, whereas for the electroformed one, a uniform current distribution nearly occupying the whole electrode area can be clearly observed. Therefore, we can safely conclude that the resistive switching is dominated by the bulk switching mechanism, for example, a purely electronic bulk effect. Note that after removing the electrodes, bulges can be clearly observed around the edge of the region previously occupied by the electrodes. The bulges are likely dominated by TiO_x since compared with the central area of the Ti electrode, the electrode margin is apt to be oxidized to TiO_x in air.[33] TiO_x is difficult to be removed by adhesive tap compared with Ti. Given that the tape adhering to TiO_x is also difficult to be removed, the bulges are most likely composed of TiO_x and tape.

To further understand the switching mechanism of Ti/ZnO/Pt, the *I*–*V* curves of electroforming, RESET and SET processes were replotted in double-logarithmic scale, as shown in Figs. 1(b)–1(d), respectively. Linear fitting results suggest that the charge transport behavior in both ON and OFF states is in good agreement with the trap-controlled space charge limited conduction (SCLC) mechanism, which consists mainly of two portions: the Ohmic region ($I = V/R$, i.e., $I \propto V$, where R is the resistance) and the modified Child's law (or, more exactly, Mott-Gurney law) region ($I = (9s\varepsilon_0\varepsilon_r\mu_n / 8d^3)\theta V^2$, i.e., $I \propto V^2$, where s is the device area, d is the film thickness, μ_n is the electron mobility, ε_0 is the permittivity of free space, ε_r is the static dielectric constant, $\theta = p/(p + p_t)$, where p is the density of free electrons and p_t is the density of trapped electrons).[34–37] The SCLC is controlled by single shallow traps,[35] e.g., V_O or Zn_i in ZnO. From Fig. 1(d), we see that during the SET process, a large number of shallow traps are filled at ~0.9 V and the current directly switches to the trap-filled (partially) SCLC (note that the device is not in a trap-free state, since its resistance can be further reduced by using a higher CC, as will be discussed in the following text). In the voltage-decreasing sweep, the current decreases as $I \propto V^2$ and no steep current drop was observed, indicating that the trap-filled (partially) SCLC state can be kept. However, during the Forming process (Fig. 1(b)), a gradual current increase (slope ~8) was observed before switching indicating the existence of traps exponentially distributed in the band gap ($I = (sq^{1-l}\mu_n N_c/d^{2l+1})\,((2l+1)/(l+1))^{l+1}(\varepsilon_0\varepsilon_r l/N_t(l+1))^l V^{l+1}$, i.e., $I \propto V^{l+1}$, where s is the device area, d is the film thickness, μ_n is the electron mobility, ε_0 is the permittivity of free space, ε_r is the static dielectric constant, q is the electronic charge, N_c is the density of the states in the conduction band, N_t is the total density of traps, and $l = T_c/T$, where T_c is a characteristic temperature related to the trap distribution).[35] Then, for

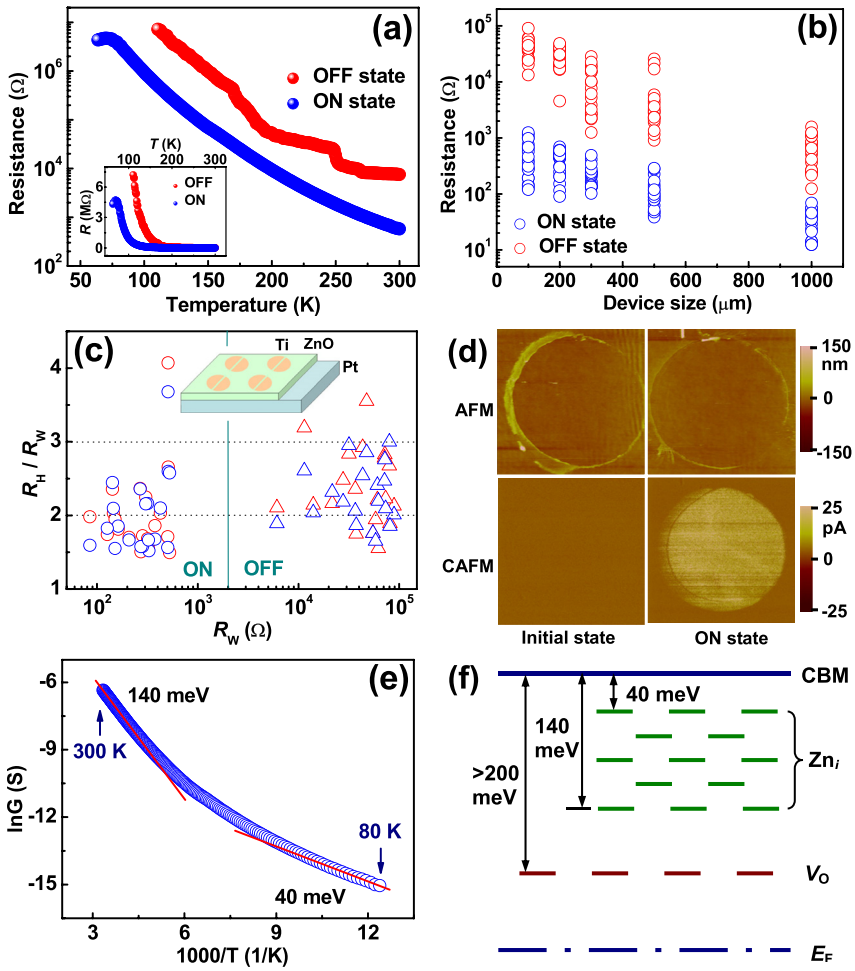

FIG. 2. (a) Resistance versus temperature plots for Ti/ZnO/Pt in ON and OFF states. The inset shows the plots in linear scale. (b) Device size dependence of the resistance in ON and OFF states for Ti/ZnO/Pt. For each size, 20 ON state and OFF state resistance values measured from five devices were plotted. The resistance values were read at 0.1 V. During the measurement, CC (SET) and the stop voltage (RESET) were set to be 10 mA and −1.5 V, respectively. (c) Comparison of R_W and R_H. The top electrodes were cut into half using a tungsten probe. The inset shows the schematic configuration for the divided devices. The resistance values were read at 0.1 V. (d) AFM and CAFM images for the pristine device (initial state) and the electroformed device (ON state). The electroforming voltage and CC are 3.8 V and 10 mA, respectively. The Ti top electrodes were removed by adhesive tape. A read voltage of 2 V was applied during the scan. The scan size was $45 \times 45\ \mu m^2$. (e) Arrhenius plot of the ON state conductance calculated from (a) in the temperature range of 80–300 K. Estimated activation energies at 300 and 80 K are also shown. (f) Schematic energy level diagram of intrinsic defects in ZnO thin films. E_F represents the Fermi energy. Herein, for simplicity, only V_O and Zn_i with low formation enthalpies were taken into account while neglecting other intrinsic defects with high formation enthalpies such as zinc vacancies and oxygen interstitials.[39,40]

the RESET operation (Fig. 1(c)), the carrier transport mode changes from trap-filled (partially) SCLC to conduction controlled by traps with exponential distribution in energy (slope ∼ 8, i.e., $l \sim 7$). Therefore, the bipolar resistive switching observed in Ti/ZnO/Pt memristive devices can be ascribed to a carrier trapping/detrapping in ZnO films. The non-volatile nature in trap-filling and trap-defilling processes may be due to strong electron correlation.[36]

To obtain the trap energy levels, the experimental data in Fig. 2(a) were replotted according to the modified Arrhenius equation, as shown in Fig. 2(e). Given a large resistance fluctuation in the temperature range of 160–300 K for the OFF state, only the ON state data in the temperature range of 80–300 K were replotted. An obvious deviation from linearity indicates that no single shallow level defects but a set of defects with a certain energy level distribution (e.g., exponential distribution) account for the conduction. It is well known that V_O and Zn_i are the most important intrinsic donor defects in ZnO. The defect level of V_O is situated at >200 meV below the conduction band minimum (CBM), whereas Zn_i has much shallower energy levels, thus accounting for the intrinsic *n*-type conduction.[38–40] Given an approximate linear relationship around 300 and 80 K, the activation energies at 300 and 80 K were estimated to be 140 and 80 meV, respectively. These activation energies correspond to Zn_i ionization levels. Figure 2(f) shows the schematic energy level diagram of V_O and Zn_i in ZnO thin films. It could be deduced that the injected electrons are first trapped by V_O and then by Zn_i likely with exponential distribution in energy. The trap density N_t can be estimated from the trap filling limit voltage V_T ($V_T \approx 8qN_t d^2/9\varepsilon_0\varepsilon_r$). V_T and ε_r values are ∼1.5 V (see Fig. 1(a) or Fig. 1(b)) and 8.75,[41] respectively. Then, N_t is calculated to be about $8.2 \times 10^{16}\,cm^{-3}$. It has been found that the devices prepared from the same batch of ZnO have a narrow distribution of switching voltages, whereas the devices from different batches of ZnO show a wide switching voltage distribution. The electroforming voltage mostly ranges from 1.5 to 6.8 V corresponding to an N_t distribution in the range of 8.2×10^{16}–$3.7 \times 10^{17}\,cm^{-3}$ in ZnO. The SET and RESET voltages are mostly in the

range of 0.9–3.1 V and −0.7 to −2.7 V, respectively. Herein, the RESET voltage is defined as the voltage at which the absolute value of current starts to decrease.

Figure 3 shows *I*–*V* characteristics of Ti/ZnO/Pt measured by a modified voltage sweep. First, a continuous RESET process was performed with a consecutive increase of the stop voltage amplitude from −1.1 to −2 V. Then, a continuous SET process was performed with an increase of CC from 0.1 to 4 mA. The left and right insets display the replotted *I*–*V* curves of the continuous RESET and SET processes in double-logarithmic scale, respectively. The linear fitting results are also shown, confirming the SCLC mechanism for both RESET and SET processes.[34–37] We conclude from Fig. 3 that the carrier trapping/detrapping level in Ti/ZnO/Pt can be controllably adjusted by regulating the CC level (SET) or stop voltage (RESET). It indicates that the Ti/ZnO/Pt memristive device could be used to emulate synaptic behavior.

Figure 4 shows a gradual increase of the device conductance by using positive voltage pulses with increasing CC from 0.1 to 10 mA, and subsequent gradual decrease of the conductance by using negative pulses with increasing voltage amplitude from −1 to −2 V. Although an abnormal conductance increase occurs around ~93rd pulse likely due to an occasional current oscillation, the results indicate that multi-level conductance states can be obtained by varying the CC level or voltage amplitude. The conductance increasing process is current-controlled, while the conductance decreasing process is voltage-controlled. As applying a positive pulse with amplitude exceeding the SET voltage (e.g., +5 V), a large number of electrons are injected into ZnO from the bottom electrode (Pt). Some of the injected electrons are consumed by traps (e.g., oxygen vacancies) and the others enter the conduction band of ZnO contributing to the conduction. CC plays an important role in controlling the electron injection. At each CC, it is likely that some of the unfilled traps are filled and the others remain unfilled since the device conductance can be further increased by using a higher CC. It deserves noting that, in Fig. 2(b), although the *I*–*V* measurements were conducted with the same CC, we cannot conclude that the same number of electrons are injected into ZnO for each device size. The same CC implies approximately the same number of

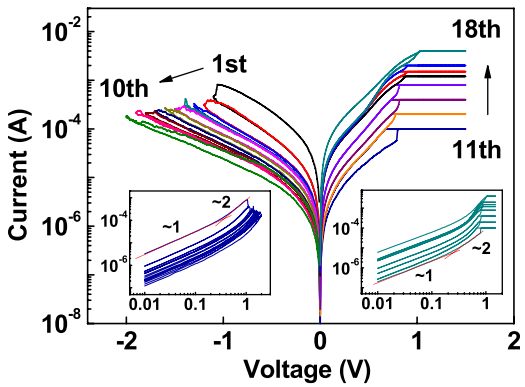

FIG. 3. *I*–*V* characteristics of Ti/ZnO/Pt measured by a modified voltage sweep. The insets show the replotted *I*–*V* curves of the continuous RESET and SET processes in double-logarithmic scale and the linear fitting results. The corresponding slopes for different portions are also shown.

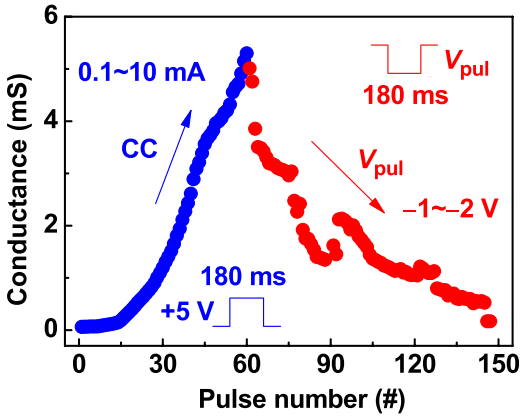

FIG. 4. Gradual increase of the device conductance by using positive voltage pulses with increasing CC and gradual decrease of the conductance by using negative pulses (V_{pul}) with increasing voltage amplitude. The conductance values were read at 0.1 V 1 s after the pulses. Herein, the consecutive increase of CC was implemented by a series connected transistor.

electrons entering the conduction band of ZnO (noting that the current runaway between two successive sampling events in the DC sweep cannot be controlled, and hence the overall compliance current value does not guarantee exact number of electrons entering the conduction band). However, different device size indicates a different number of trap sites in ZnO likely causing a different number of trapped electrons. For the OFF state, we can see from Fig. 2(b) that the average resistance decreases by about 2 orders of magnitude as increasing the device size from 100 to 1000 μm, i.e., 2 orders of magnitude increase in the device area, demonstrating that the trap filling ratio (the number of filled traps/the total amount of traps) is almost the same in the OFF state at each device size; while in the case of the ON state, only an order of magnitude decrease in the average resistance was observed. For the filling ratio in the ON state, there may exist three circumstances. First, it is the same at each device size. In this case, the average resistance will reduce by 2 orders of magnitude as increasing the device size from 100 to 1000 μm, similar to the case of the OFF state. Second, it increases with the device size. Then, the average resistance will reduce by more than 2 orders of magnitude. Third, it decreases with the device size. In such case, the average resistance reduces by less than 2 orders of magnitude. Given the experimental results in Fig. 2(b), the first and the second circumstances can be safely excluded. Therefore, we conclude that at the same CC (SET) and stop voltage (RESET), the ON state shows a trap filling ratio decreasing with the device size, whereas for the OFF state, it is independent of the device size. It is worth noting that the above discussion about the trap filling ratio is based on the device size dependence of the resistance in ON and OFF states, which is only indirect evidence. Further studies will be necessary to provide direct support for this hypothesis.

In memristive devices, continuous conductance programmability is analogous to the biological synaptic weight modulation, i.e., synaptic plasticity.[16] Synaptic plasticity is believed to account for learning and memory of the biological brain.[1] STDP, an important form of Hebbian learning, has attracted tremendous interest in the field of neuroscience.[42,43] According to STDP, the synapse potentiates if a pre-neuron spikes before a post-neuron ($\Delta t > 0$), and the synapse depresses if a post-

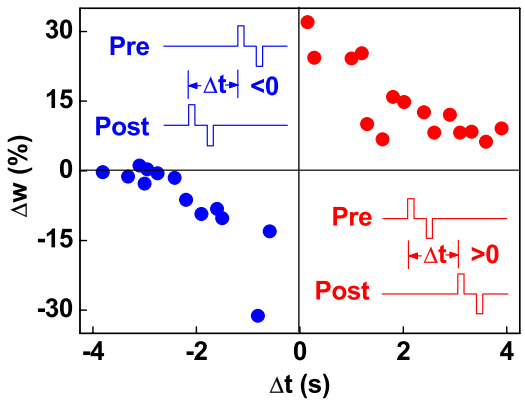

FIG. 5. Emulation of STDP learning rule in the Ti/ZnO/Pt memristive device. The insets schematically illustrate the spike scheme. The pulse pair comprises a positive and a negative voltage pulse with amplitude of 5 V and width of 180 ms. The interval between the two pulses is 500 ms. During the emulation, CC was set to be 1 mA. The conductance values were read at 0.1 V 100 s after the spikes. Note that the actual device stimuli may not be the pulses with rectangular shape since a CC has been set.

neuron spikes before a pre-neuron ($\Delta t < 0$). A smaller spike timing difference leads to a larger increase (or decrease) in synaptic weight. Such STDP learning rule was emulated in Ti/ZnO/Pt, as shown in Fig. 5. The same pulse pair was applied to the top electrode and bottom electrode of Ti/ZnO/Pt at different timing, serving as the pre-synaptic spike and post-synaptic spike, respectively. The device conductance is regarded as the synaptic weight, and then the conductance change is equivalent to the synaptic weight change (Δw). We can see from Fig. 5 that the emulation results obey the STDP learning rule. The synaptic potentiation ($\Delta w > 0$) was achieved as $\Delta t > 0$, and the synaptic depression ($\Delta w < 0$) was obtained as $\Delta t < 0$. Furthermore, a smaller $|\Delta t|$ results in a larger $|\Delta w|$. It is worth noting that the synaptic weight change is asymmetric, especially for $|\Delta t| > 2$ s. It may be due to the difference between the activation energies for electron trapping and detrapping of the trap sites in ZnO, which likely originates from the presence of an asymmetric potential barrier of traps with respect to bias polarity.[44] It may also account for the asymmetry of the *I–V* curves with respect to bias polarity, as shown in Fig. 1(a).

In conclusion, the resistive switching of Ti/ZnO/Pt memristive devices was found to result from the carrier trapping/detrapping process in ZnO films. Multi-level conductance states were realized in such devices by regulating the current compliance level (SET process) or voltage amplitude (RESET process). Based on Ti/ZnO/Pt devices, STDP learning rule was implemented.

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