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Threshold voltage tuning in a-IGZO TFTs with ultrathin SnO_x capping layer and application to Depletion-Load Inverter

Mei Wang, Lingyan Liang, Hao Luo, Shengnan Zhang, Hongliang Zhang, Kashif Javaid, and Hongtao Cao

Abstract—**Tunable threshold voltage of a thin-film transistor (TFT) is highly desirable for designing multifunctional electronic circuits. In this work, an ultrathin SnO_x capping layer was adopted to modify the threshold voltage of bottom-gate amorphous indium-gallium-zinc-oxide (a-IGZO) TFTs. A threshold voltage shift from 15.2 to -9.0 V was observed as the SnO_x thicknesses increased from 0 to 19 nm, accompanying by a sizable increase of the intrinsic electron concentration in the channel layer. It was believed that the SnO_x capping layer can extract loosely bound oxygen from the a-IGZO, which was supported by the SnO_x composition variation with its thickness. Combining an uncovered a-IGZO TFT with a SnO_x capped a-IGZO TFT, an Enhancement/Depletion inverter with a voltage gain up to 45.9 was successfully demonstrated.**

Index Terms—**Amorphous indium-gallium-zinc-oxide (a-IGZO), Tin oxides (SnO_x), thin-film transistor, inverter, capping layer.**

I. INTRODUCTION

Amorphous indium-gallium-zinc-oxide thin film transistor (a-IGZO TFT) arrays have attracted ever-increasing attention as backplanes in active matrix liquid crystal displays (AMLCDs) or active-matrix organic light-emitting diode displays (AMOLEDs) [1]. Meanwhile, there have been various attempts to use a-IGZO TFTs in logic circuits [2], photodetectors [3], memory devices [4], bio-sensors [5] and so on. Oxide-based inverters, acting as "built blocks" of logic circuits, are extensively studied in recent years. Complementary inverters using p-type SnO_x/n-type In_2O_3 [6] or hybrid n-type IGZO/p-type pentacene [7], complementary-like inverters based on ambipolar SnO TFTs [8], resistor-loaded inverters, and enhancement/depletion (E/D) inverters have already been demonstrated. Among them, the E/D inverter utilizing two n-channel TFTs with different threshold voltage (V_{th}) is a promising supplementary technology for complementary logic circuits.

In order to tune the V_{th} difference as much as possible, various methods have been reported, such as varying the active layer thickness [9], adopting distinct active layer material [10], selectively inducing the negative bias illumination temperature stress (NBITS) to the load TFT [11], and applying a constant positive bias on the top gate [12], etc. However, these inverters demonstrated either low voltage gains (< 40) or rather complicated fabrication processes, limiting their applications.

Passivation layers with a thickness larger than 100 nm were generally deposited to improve the electrical stability of TFTs. However, various passivation layers (such as SiO_x [13], MgF_2 [14]) fabricated in vacuum system were found to not only shift the V_{th} negatively but also induce a very large off-current. In this letter, by introducing a thin SnO_x capping layer onto the uncovered back channel surface (Bottom-gate top-contact TFT structure), tunable V_{th} of a-IGZO TFTs was achieved without scarifying other device properties. Then an E/D inverter with a voltage gain up to 45.9 was constructed by connecting an uncovered a-IGZO TFT with a SnO_x-covered one. This E/D inverter has a relatively simple fabrication process, manifesting a good application potential for the future logic circuits based on oxide semiconductors.

II. DEVICE STRUCTURE AND FABRICATION

Bottom-gate transistors using a-IGZO as the channel layer were fabricated at room temperature. A-IGZO thin films were deposited on SiO_2 (100 nm)/Si substrate by RF sputtering, applying a 2 in. IGZO target (1:1:1 mol. % of In_2O_3:Ga_2O_3:ZnO) at a power of 80 W. The base pressure of the chamber was less than 4×10^{-4} Pa. 30 nm channel films were deposited in a 100% Ar atmosphere at a constant pressure of 0.21 pa (Ar flow = 6 sccm). Afterwards, a shadow mask was used to define the channel length and width of 400 and 800 μm, respectively. Ti/Au (30 nm/30 nm) source/ drain electrodes were deposited by electron beam evaporation using the second shadow mask. The devices were then annealed at 250 ^oC in the air for 1 hour. Amorphous SnO_x films with different thicknesses were deposited at room temperature onto the back channel surface of the fabricated a-IGZO TFTs through electron beam evaporation (Deposition details were reported elsewhere [15]). Finally, an E/D inverter was fabricated by connecting a bare TFT as the driver and an 8.5 nm SnO_x-covered TFT as the load. The fabricated TFTs and inverters are finally passivated by SU-8 photo-resist to improve the device stability.

III. RESULTS AND DISCUSSION

Surface morphologies of the a-IGZO films covered with or without amorphous SnO_x films were investigated using atomic force microscope (AFM), as seen in Figure 1. These surfaces are apparently smooth without obvious embossment. As shown in figure 1(d), the root mean square (RMS) roughness as a function of the SnO_x thickness is ranging from 0.50-0.60 nm, indicating that the deposition of the SnO_x

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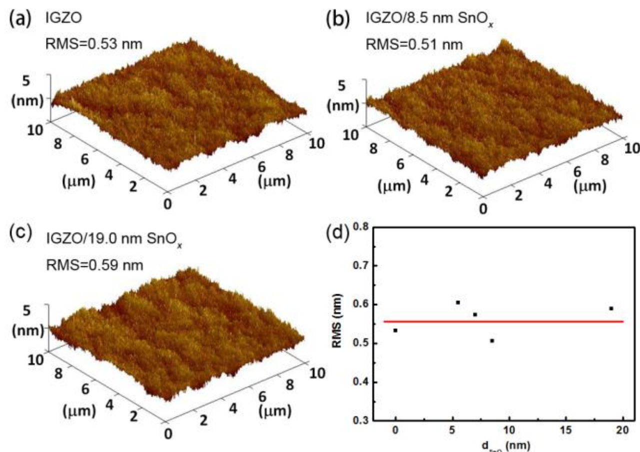

Fig. 1. (a), (b) and (c) AFM images of the a-IGZO films covered with 0, 8.5 and 19.0 nm SnO_x. (d) The RMS values vs. SnO_x thicknesses .

capping layer has a marginal influence on the surface morphology of the a-IGZO surface.

The electrical properties of the devices were obtained at room temperature in the dark using a semiconductor parameter analyzer. Figure 2(a) shows the transfer characteristics of the TFTs with varied SnO_x thicknesses (d_{SnOx}), and the main electrical parameters are summarized in Table 1. The uncovered TFT shows a positive turn-on voltage (V_{on}) and V_{th}, indicating that the TFT works in an enhancement mode. Interestingly, the introduction of SnO_x capping layer triggers the conversion from the enhancement mode to depletion one. As d_{SnOx} increases from 0 to 19 nm, the V_{on} changes from 8.0 to -18.0 V, while the V_{th} shifts from 15.2 to -9.0 V. The negative-shift of both V_{on} and V_{th} implies that the intrinsic electron concentration in the channel layer increases as d_{SnOx}, which is confirmed by the Hall-effect measurement. Both the bare a-IGZO film and SnO_x capped a-IGZO film with d_{SnOx} =2.5 nm have high resistivity beyond the limitation of the Hall measurement. The films with d_{SnOx} =5.5-8.5 nm show electron concentrations around 10^{16}-10^{17} cm^{-3}. When d_{SnOx} is up to 19 nm，the film has an electron concentration up to 2.7×10^{18} cm^{-3}, leading to relatively high off and on currents of the corresponding TFT. As a result, the carrier concentration variation-induced tunable V_{th} of a-IGZO TFTs was achieved in this study, which facilitates us to construct E/D inverters. Additionally, It should be noted that the TFTs with d_{SnOx} = 5.5 & 7.0 nm show a clear subthreshold hump in the transfer curves, substantially increasing the subthreshold slope (*S.S*). At d_{SnOx} = 8.5 nm，however, the subthreshold hump almost disappears. With further increasing d_{SnOx}, the *S.S* rebounds back due to the high intrinsic electron concentration. In this case, it is difficult for the voltage to switch the device on and off quickly.

Figure 2(b) shows the variation in V_{th} shift (ΔV_{th}) as a function of d_{SnOx}. The devices present more dramatic increase in ΔV_{th} in the range of $d_{SnOx} \leq 8.5$ nm. With further increasing d_{SnOx}, the rate of increment gradually slows down. These results exhibit a strong dependence of ΔV_{th} on d_{SnOx}, meaning that the shift is highly related to the capping layer property (such as surface morphology and chemical composition, etc.). The AFM results have demonstrated that the film surface morphologies show small changes with d_{SnOx}. Next, the SnO_x chemical component variations of the capping layer with its thickness will be further investigated to clarify the origin of the V_{th} shift.

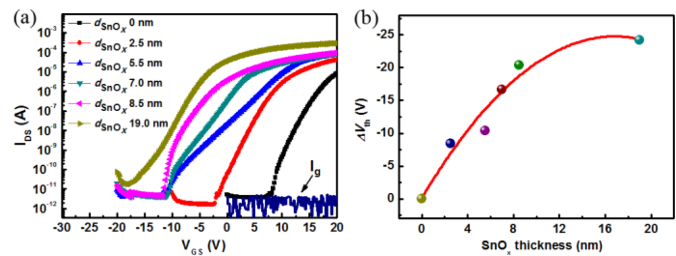

Fig. 2. (a) The transfer curves of a-IGZO TFTs with SnO_x capping layers in different thicknesses, V_{DS}=10 V. (b) The dependence of ΔV_{th} on d_{SnOx}, and $\Delta V_{th} = V_{th}$ ($d_{SnOx} \neq 0$) - V_{th} ($d_{SnOx} = 0$).

TABLE I
ELECTRICAL PARAMETERS OF A-IGZO TFTS WITH OR WITHOUT SnO_x CAPPING LAYERS

d_{SnOx} (nm)	V_{on} (V)	V_{th} (V)	μ_{FE} (cm^2/Vs)	S.S (V/decade)	$I_{on/off}$ ratio
0	8.0	15.2	9.59	0.707	2.3×10^6
2.5	-2.3	6.8	10.06	1.220	2.0×10^7
5.5	-11.1	4.8	11.16	1.333	1.9×10^7
7.0	-11.1	-1.5	9.55	0.672	1.9×10^7
8.5	-11.8	-5.2	10.34	0.475	1.9×10^7
19.0	-18.0	-9.0	15.00	1.177	1.7×10^7

X-ray photoelectron spectroscopy (XPS) was performed to analyze the chemical states of the SnO_x capping layers. The binding energy data were calibrated with respect to the C 1s signal of ambient hydrocarbons (C-H and C-C) centered at 284.8 eV. To obtain the depth-profile chemical composition of the SnO_x, high dose of argon ions (Ion energy of 2 KeV, current density of 5 μA/cm^2 roughly) were utilized to sputter away the top surface layer of SnO_x.

At d_{SnOx} = 5.5 nm, the elemental information of both the SnO_x capping layer and the a-IGZO underlayer was detected, so no Ar^+ ion etching process was carried out in this case. The Sn 3d spectrum of the 5.5 nm SnO_x shown in figure 3(a) depicts a spin-orbit doublet peak located at 486.6 eV (Sn^{4+} $3d_{5/2}$) and 495.0 eV (Sn^{4+} $3d_{3/2}$), matching very well with those reported for SnO_2 [16]. This indicates that the 5.5 nm SnO_x layer is totally oxidized into SnO_2 after exposure to the air. At d_{SnOx} = 8.5 nm, the Sn 3d spectra of the surface and etched layer were obtained, as illustrated in figure 3(b) and (c), respectively. In figure 3(b), it is manifested from the peak deconvolution that the SnO_2 phase is mixed with the SnO one (485.9 eV and 494.3 eV for $Sn^{2+}3d_{5/2}$ and $Sn^{2+}3d_{3/2}$, respectively [16]). After etching, however, the spectrum only presents a spin-orbit doublet peak which can be assigned to SnO. Similar to the 8.5 nm case, the topmost surface layer of the 19 nm film is also consisted of SnO_2 and SnO mixed phases, but with more SnO content (Fig. 3(d)). After etching, the SnO and metallic Sn phases are present, as depicted in figure 3(e), where a spin-orbit doublet peak assigned to SnO with two small shoulders centered at 484.4 eV (Sn^0 $3d_{5/2}$) and 492.8 eV (Sn^0 $3d_{3/2}$) is clearly illustrated.

It is speculated that the negative shift of V_{th} with increasing d_{SnOx} is related to the composition evolution of the SnO_x layers. The SnO_x film deposited by e-beam evaporation generally contains SnO and Sn species [15], and both of the species are good oxygen killers. In our case, the oxygen is coming from either air or the a-IGZO underlayer that has loosely bound oxygen [17]. When d_{SnOx} =5.5 nm, the ultrathin film might be oxidized into SnO_2 quickly by the O_2 and H_2O in the air, and the oxygen provider coming from the a-IGZO

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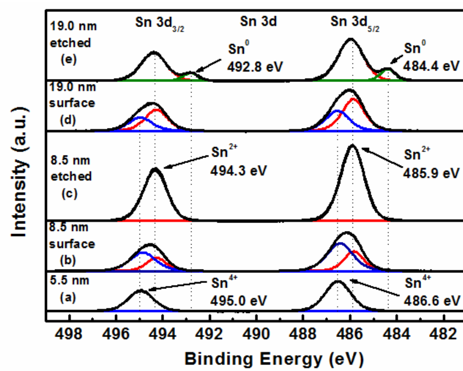

Fig. 3. The Sn 3d core level XPS spectra of SnO_x capping layers with different thicknesses.

underlayer cannot be ruled out of course. It's well known that the oxygen lose in oxide semiconductors would result in the increase of the electron concentration due to the increase of oxygen vacancies. As a result, the V_{th} of 5.5 nm SnO_x covered a-IGZO TFT is shifted negatively. The thicker of the SnO_x film, the more easily of the loosely bound oxygen from a-IGZO getting access to oxidize the SnO and/or Sn spices in the inner sub-layer of SnO_x, leading to more oxygen deficiencies and higher electron concentration in the channel layer. This speculation is matching well with the experimental results, i.e., the continuous negative-shift of V_{th} with increasing d_{SnOx}.

One may suggest that the formation of the SnO_x/IGZO bilayer semiconductor structure could be another reason to account for the negative-shift of V_{th}, since SnO_x is a semiconductor. However, amorphous SnO_x films deposited by e-beam evaporation are of high resistance according to our previous reports [15]. It should be noted that the subsequently deposited ultra-thin SnO_x capping layer could not form good contact with the source and drain electrodes. So, the SnO_x film is believed to be an insulator capping layer rather than the back channel layer.

Interestingly, the field-effect mobility is generally improved with increasing d_{SnOx}, as manifested in Table 1. The negative shift of V_{th} along with the increased field effect mobility was also reported elsewhere [18], in which the usage of Ca/Al capping layer onto the back channel of a-IGZO TFT could eliminate the loosely bound oxygen species and in the a-IGZO channel. The removal of loosely bound oxygen in IGZO reduces the defect density, lowers the potential barrier above mobility edge, and then enhances electron mobility. [18]. For our case, the improved mobility and V_{th} negative shift were achieved with compromising the *S.S* factor, which is quite complicated and need further investigations.

In order to improve the device stability, SU-8 resist was chosen to passivate the TFTs in this research. The bias stability of the TFTs with or without SU-8 was carried out. Figure 4 (a) and 4 (b) show the transfer curves of a typical TFT (with d_{SnOx} = 8.5 nm) as a function of bias stress duration. A negative shift of 2.2 V and 0.6 V after 3600 seconds bias stress was observed for the unpassivated and SU-8 passivated TFTs, respectively. The above comparison indicates that not SnO_x layer but the SU-8 plays the passivation layer role to stabilize the device performance.

For the fabrication of the E/D inverter, the TFT with d_{SnOx} = 8.5 nm was chosen as the load, because of its better device

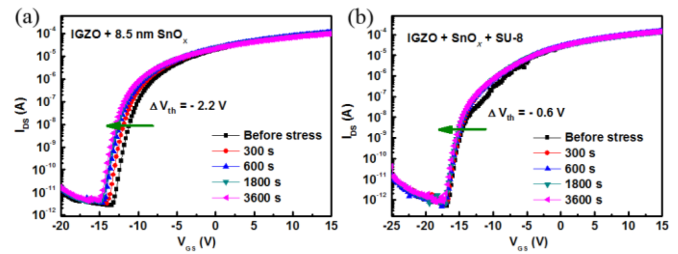

Fig. 4. (a) and (b) Transfer curves as a function of bias stress duration for the unpassivated and SU-8 passivated 8.5 nm SnO_x-capped a-IGZO TFTs. The bias stress conditions is V_G=5V.

performance (sound field-effect mobility, steep *S.S* and huge V_{th} difference with respect to the SnO_x uncapped device). Figure 5(a) shows the block diagram of the fabricated inverter. The V_{th} of the driver (without SnO_x) and load (8.5 nm SnO_x-capped) TFTs is 4.0 V and -11.1 V, working in a depletion mode (D-mode) and an enhancement mode (E-mode) respectively, as manifested in figure 5(b). The voltage transfer curve (VTC) of the inverter was obtained at a supply voltage V_{DD} of 5V, 10 V and 15 V. The VTC and the corresponding voltage gain are shown in figure 5(c) and 5(d). The inset of figure 5(c) is the equivalent circuit diagram of the logic inverter. The operation of the inverter can be described as, when V_{in} is low (e.g., V_{in} = 1 V), the drive device would be at 'OFF' state while the load device working at 'ON' state. A low current flows through the load device, resulting in a minimal voltage drop across the load device. The above progress could account for the high output of the inverter (almost 15 V). On the contrary, if V_{in} is high (e.g., V_{in} = 8 V), both of the two TFTs are at 'ON' state. A high current flows through the load device, leading to a low output (almost 0 V). The voltage gain of the inverter shown in figure 5(d) is about 5.9, 19.5 and 45.9 at V_{DD} = 5, 10, 15 V, respectively, which is competitive with the previous report [19]. In addition, the fabrication process of this inverter is very similar to that of the conventional a-IGZO TFTs except for one additional capping step, opening up a way for the fabrication of low-cost and easy-fabrication microelectronic devices.

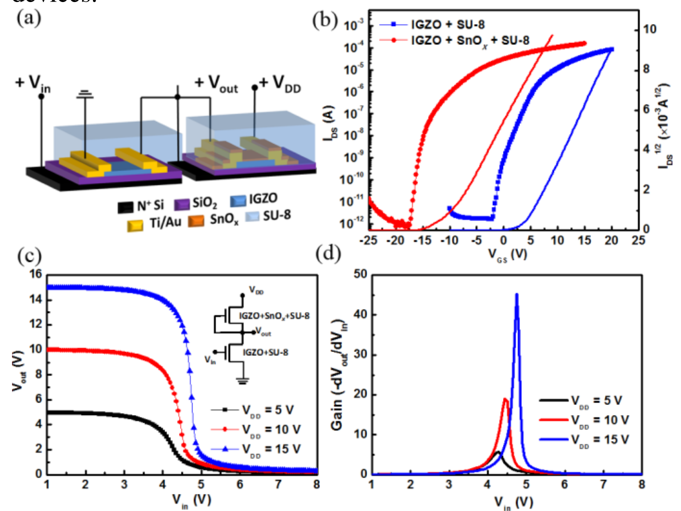

Fig. 5. (a) The device structure layout of the NMOS E/D inverter. (b) Transfer curves of 8.5nm SnO_x capped and the uncapped IGZO TFT, and both TFTs were passivated by SU-8. (c) Voltage transfer curves of the inverter measured at supply voltage V_{DD} of 5V, 10 V and 15 V (The inset shows the inverter circuit diagram). (d) Corresponding voltage gains (–dV_{out}/dV_{in}) of the inverter.

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