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Control of Ambipolar Transport in SnO Thin-Film Transistors by Back-Channel Surface Passivation for High Performance Complementary-like Inverters

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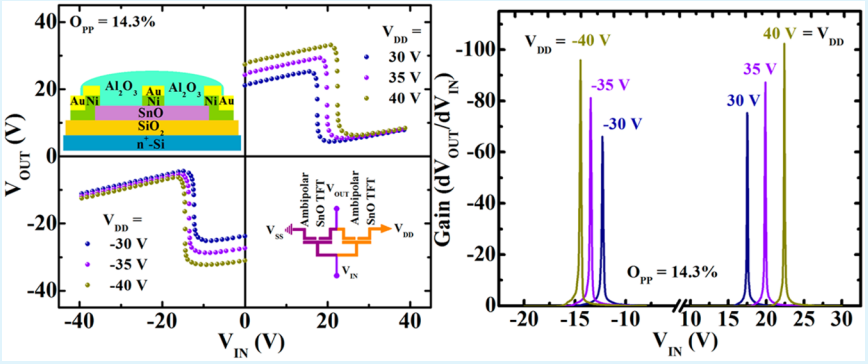
Supporting Information



ABSTRACT: For ultrathin semiconductor channels, the surface and interface nature are vital and often dominate the bulk properties to govern the field-effect behaviors. High-performance thin-film transistors (TFTs) rely on the well-defined interface between the channel and gate dielectric, featuring negligible charge trap states and high-speed carrier transport with minimum carrier scattering characters. The passivation process on the back-channel surface of the bottom-gate TFTs is indispensable for suppressing the surface states and blocking the interactions between the semiconductor channel and the surrounding atmosphere. We report a dielectric layer for passivation of the back-channel surface of 20 nm thick tin monoxide (SnO) TFTs to achieve ambipolar operation and complementary metal oxide semiconductor (CMOS) like logic devices. This chemical passivation reduces the subgap states of the ultrathin channel, which offers an opportunity to facilitate the Fermi level shifting upward upon changing the polarity of the gate voltage. With the advent of *n*-type inversion along with the pristine *p*-type conduction, it is now possible to realize ambipolar operation using only one channel layer. The CMOS-like logic inverters based on ambipolar SnO TFTs were also demonstrated. Large inverter voltage gains (>100) in combination with wide noise margins are achieved due to high and balanced electron and hole mobilities. The passivation also improves the long-term stability of the devices. The ability to simultaneously achieve field-effect inversion, electrical stability, and logic function in those devices can open up possibilities for the conventional back-channel surface passivation in the CMOS-like electronics.

KEYWORDS: *SnO, back-channel, passivation, ambipolar thin-film transistors, CMOS-like inverters*

INTRODUCTION

Oxide semiconductors are utilized as the active layers in thin-film transistors (TFTs), delivering emerging applications such as transparent electronics, flexible electronics,[1−4] and so on. Transparent oxide semiconductors, as represented by amorphous indium−gallium-zinc oxide (a-IGZO), take the advantage of low processing temperature and high field-effect mobilities (>10 $cm^2/(V\ s)$) over amorphous silicon (a-Si) in switching/driving TFT applications.[1] However, to date, most oxide semiconductors are *n*-type, limiting the device function and integration. The high performance and long-term stability of *p*-type or bipolar oxide semiconductors are highly desired in order to realize the functions similar to complementary metal oxide semiconductor (CMOS) technology, in which both *n*- and *p*-type oxide semiconductors are required. So far, the oxide-based complementary circuits are mainly combined with *p*-type organic or carbon-based TFTs.[5−8] However, the incompatibility for processing diverse active materials makes the circuit

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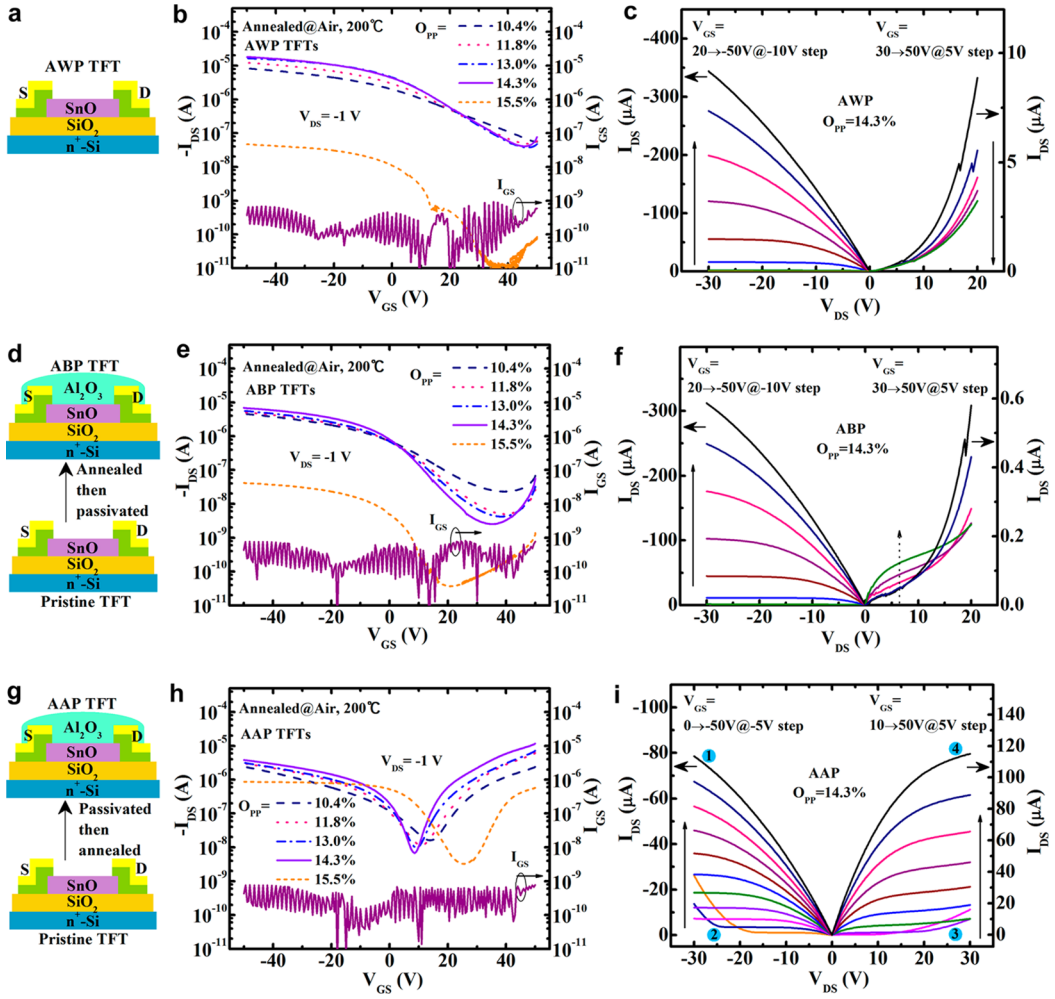

Figure 1. Device structure, transfer, and output characteristics of (a–c) AWP-SnO TFTs, (d–f) ABP-SnO TFTs, and (g–i) AAP-SnO TFTs.

design and integration more complicated and unacceptable for practical applications. Therefore, it is imperative to excavate the cache of *p*-type or bipolar oxide semiconductors to allow fabrication of more compact CMOS devices.

Tin monoxide (SnO), possessing the tetragonal PbO-type (*P*4/*nmm*) crystallographic structure, is known to be a *p*-type semiconductor.[9] It has a large direct optical bandgap of ∼2.7 eV,[10,11] along with a small indirect fundamental bandgap of ∼0.7 eV.[10,12] The narrow fundamental bandgap of SnO allows the Fermi level to be shifted from the valence band maximum (VBM) to the vicinity of the conduction band minimum (CBM) via element doping or electrostatic doping. Quackenbush et al. found that SnO has a large electron affinity of ∼3.7 eV (the energy difference between the vacuum level and the CBM) and a small ionization potential of ∼4.4 eV (the energy difference between the vacuum level and the VBM).[12] According to the doping criteria for oxide semiconductors,[13] the large electron affinity and small ionization are in favor of bipolar doping. In fact, the bipolar conduction of SnO films and TFT devices has already been achieved through Sb-doping[14] and electrostatic doping.[15,16] However, most reported SnO TFTs exhibited unipolar *p*-type.[10,11,17−20] Complementary inverters composed of spatially separated unipolar *p*-type SnO_x TFTs and *n*-type (In_2O_3, IGZO, etc.) TFTs were also demonstrated, but the voltage gains were relatively low (∼1.7−11).[3,21,22] The ambipolar operation of SnO TFTs was first reported by Nomura et al.[15] They demonstrated the CMOS-like inverter with *p*- and *n*-type transistor integrated in a single SnO channel layer. However, the asymmetry in hole and electron transport in the CMOS-like inverter limited the voltage gain. Recently, ambipolar SnO TFTs with balanced electron and hole mobilities were reported by our group, and the ambipolar TFTs based inverters exhibited a maximum voltage gain of ∼30.[16]

Despite the advance of SnO-based electronic devices, the conversion mechanism from unipolar *p*-type to ambipolar working mode still remains unclear because SnO is a typical *p*-type semiconductor. Taking a step further, in this work, we present a technical strategy for manipulation the minority carrier to realize strong inversion condition in the ultrathin SnO channel by passivating the back-channel surface to reduce the surface states, which can open a new direction for oxide-semiconductor-based emerging electronics to enable compact logic circuits.

EXPERIMENTAL METHODS

Film Growth and Characterization. SnO films were deposited by reactive rf magnetron sputtering using a metallic Sn target. The deposition was conducted at a power of 40 W at room temperature under a pressure of 0.22 Pa. The oxygen partial pressure [$O_{PP} = P_{O_2}/(P_{O_2} + P_{Ar})$] during the deposition was varied from 10.4 to 15.5%. The Al_2O_3 passivation layer was also deposited by magnetron sputtering

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with an Al_2O_3 ceramic target at a power of 120 W. The Al_2O_3 films were deposited at a deposition pressure of 0.22 Pa at room temperature. Thin film thickness was characterized by spectroscopic ellipsometry (SE, J.A. Woollam, Inc.). The chemical composition was investigated by X-ray photoelectron spectroscopy (XPS) using Al−Kα radiation (Kratos Analytical, Ltd., U.K.). Carrier concentrations were obtained from Hall-effect measurements using the van der Pauw method (HL5500). For the Hall measurements of Al_2O_3-capped SnO films, the contact electrodes and Al_2O_3 layers were patterned by two different types of shadow masks, respectively.

Device Fabrication and Characterization. Bottom-gate TFTs using SnO films (20 nm) as the channel layers were fabricated on thermally oxidized SiO_2/n^+-Si substrates, with the SiO_2 layer (200 nm) and the n^+-Si as the dielectric and gate electrode, respectively. The active layers and the drain/source electrodes were patterned by the shadow masks. The width-to-length ratio (W/L) of the TFTs is 6, with L = 100 μm. The Ni/Au (100/50 nm thick) films used as drain/source electrodes were deposited by electron-beam evaporation. Passivation layers patterned by shadow masks were deposited onto the back-channel surface of the bottom-gate TFTs. The annealing treatment was processed at 200 °C for 1 h in air or vacuum ambient. Characterizations of the TFTs and inverters were conducted with a Keithley 4200 semiconductor characterization system under ambient environment at room temperature in the dark.

Device Simulation. The device simulator ATLAS (Silvaco) is used to simulate the TFT characteristics and to extract the subgap density of states (DOS) of the TFTs. TCAD simulation involves a constant mobility and DOS model, which is used to simulate the characteristics of the TFTs. This model is a standard model for TFTs, and has been proven to be available for typical amorphous oxides-based TFTs such as a-IGZO or a-Si TFTs. Additional details about device simulation can be found in the Supporting Information.

RESULTS AND DISCUSSION

Conversion from Unipolar *p*-Channel to Ambipolar Mode. Bottom-gate TFTs with or without Al_2O_3 passivation layers (Figure 1a,d,g) were fabricated by using 20 nm thick SnO films as the active layers. The devices were annealed at 200 °C in ambient air to crystallize the SnO active layers to improve electrical properties. Three different processes were conducted: (1) annealing without passivation (labeled as AWP), (2) annealing before passivation (labeled as ABP), and (3) annealing after passivation (labeled as AAP). Figure 1b,e,h displays the transfer characteristics for three types of TFTs with the channel layers deposited at different oxygen partial pressure (O_{PP}). The AWP TFTs fabricated at low O_{PP} show typical unipolar *p*-channel features, while those at high O_{PP} show a specious ambipolar characteristic with a very weak *n*-channel operation. For instance, the AWP TFT at O_{PP} = 14.3% shows a *p*-channel behavior as gate-source voltage (V_{GS}) varies from 45.6 V to −50 V and a weak inversion when V_{GS} > 45.6 V. However, no *n*-channel operation is observed in the output characteristics of the device. As shown in Figure 1c, a clear pinch-off and current saturation are obtained in the negative drain-source voltage (V_{DS}) region while the drain-source current (I_{DS}) displays diode-like rectifying behavior in the positive V_{DS} region, indicating a unipolar *p*-channel feature. It seems that the AWP TFT at O_{PP} = 15.5% acts as ambipolar transistor, but it is unreliable because the I_{DS} is comparable to the gate-source current (I_{GS}) at large positive V_{GS}. Interestingly, dominated *p*-channel operation with distinct but weak inversion *n*-channel characteristics is observed for the ABP TFTs (the passivation layer of Al_2O_3 is about 10 nm), as depicted in Figure 1e. In particular, compared to the AWP TFT at O_{PP} = 14.3%, the corresponding ABP TFT displays the *n*-type inversion sign when V_{GS} > 36.1 V, with an on/off current ratio more than 20. The weak inversion is also confirmed by the output characteristics illustrated in Figure 1f, in which the three-terminal field-effect output combined with two-terminal rectifying curves are obtained in the positive V_{DS} section. More interestingly, the distinct *n*-type inversion and ambipolar operation are observed for the AAP TFTs, as illustrated in Figure 1h. In contrast to the asymmetry nature of the ABP TFTs, all the AAP TFTs display V-shaped transfer curves, revealing relatively symmetric characteristics between *n*- and *p*-channel operations. Specifically, the output curves of the AAP TFT at O_{PP} = 14.3% definitely confirm the ambipolar operation (Figure 1i), with a clear pinch-off and current saturation in both the positive and negative V_{DS} region. The output curves in the linear region are getting increased steeply as $|V_{DS}|$ increases for both the *n*- and *p*-channel operation mode, indicating that the SnO channel layer has a good contact with the source/drain electrode. In addition, the diode-like rectifying characteristics are also observed at small $|V_{GS}|$ in both the positive and negative V_{DS} region.

The key parameters of the AWP, ABP, and AAP TFTs as a function of O_{PP} are derived and summarized in the Figure 2

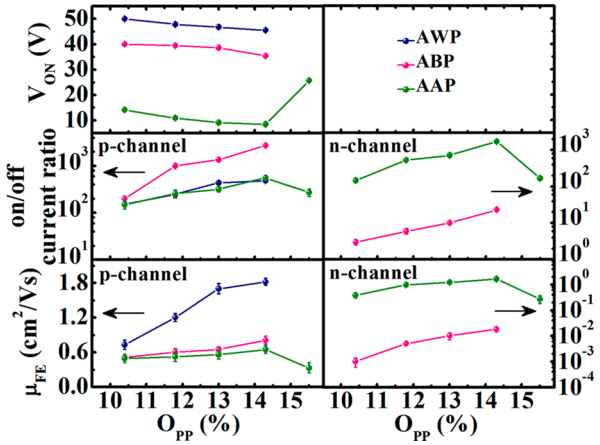

Figure 2. Typical parameters (V_{ON}, on/off current ratio, and μ_{FE}) of the SnO TFTs as a function of O_{PP}.

(the parameters of the AWP and ABP TFTs at O_{PP} = 15.5% are not available due to the trustless data in these cases). Herein, the turn-on voltage (V_{ON}) is defined as the V_{GS} value at the minimum $|I_{DS}|$ in the transfer curve, which is expected to be close to zero for the ambipolar TFT with good symmetry. In order of the AWP, ABP and AAP TFTs at each O_{PP}, the V_{ON} is getting closer to 0 V, and the on/off current ratio and linear field-effect mobilities (μ_{FE}) for the *n*-channel operation are increasing as well, revealing the improvement of ambipolar behavior. The measured results indicate that the AAP TFT at O_{PP} = 14.3% presents the best ambipolar properties in this study, with V_{ON} of 8.5 V, the on/off current ratio for the *n*- and *p*-channel operation of ∼1700 and ∼600, respectively, and the μ_{FE} for the *n*- and *p*-channel operation of ∼1.64 and ∼0.65 cm^2/(V s), respectively.

Origin of the Operation Mode Conversion. The conduction mechanism of an ambipolar TFT is analyzed on the basis of the energy band diagram. Figure 3 illustrates schematic band alignment between the channel and source/drain electrode corresponding to the four representative operation zone highlighted in Figure 1i. In zones 2 and 3, the Fermi level locates near the midgap of SnO, and thus, the

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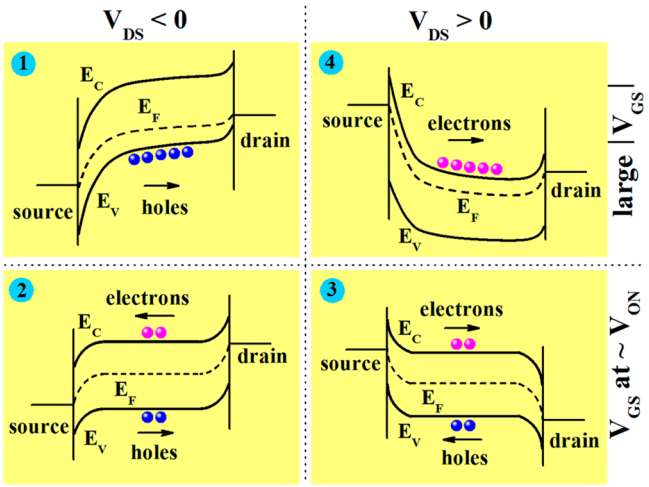

Figure 3. Schematic band diagrams for the ambipolar AAP-SnO TFTs working in different operation regimes. Zones 1 and 4: band diagrams of ambipolar SnO TFT at large $|V_{GS}|$ in the negative and positive V_{DS} region. Zones 2 and 3: band diagrams of ambipolar SnO TFT at $V_{GS} \approx V_{ON}$ in the negative and positive V_{DS} region. E_C, E_V, and E_F denotes the energy of conduction band, the energy of valence band and the Fermi level of the active layer, respectively. The blue and magneta balls represent the holes and electrons, respectively.

band bending between source/channel and drain/channel is similar to each other, resulting in S-shaped energy band. The similar barrier height leads to the equilibrium injection of the electron and hole carriers, that is, the SnO active layer becomes a hole channel in series with a electron channel, giving rise to the diode-like rectifying characteristics. This feature facilitates us to develop the multifunctional devices such as light-emitting, lasering, or light-detecting transistors.[23] For the case of zones 1 and 4, however, large $|V_{GS}|$ would push the Fermi level down to the VBM (zone 1) or up to the CBM (zone 4). A high barrier presented at the drain/channel contact would block the injection of electrons (zone 1) or holes (zone 4), while the energy band at the source/channel interface would bend upward (zone 1) or downward (zone 4), allowing the efficient injection of holes (zone 1) or electrons (zone 4), respectively. As a result, the SnO active layer would be accumulated by holes (zone 1) or electrons (zone 4) when changing the polarity and magnitude of the gate voltage, corresponding to the *p*- or *n*-channel operation of the ambipolar SnO TFT. From hole accumulation to *n*-type inversion, the Fermi level of the active layer is capable of shifting gradually and unimpededly from the VBM, via the midgap, until to the vicinity of CBM, which is the physical image to describe an ambipolar SnO TFT operation.

It should be noted that some typical oxide TFTs such as a-IGZO or ZnO TFTs can only work in the unipolar *n*-type mode, because the bandgap of these materials is too wide to give rise to minority carrier injection and accumulation. On the other hand, although SnO has a narrow bandgap which allows easy injection of both carriers; however, the above-mentioned AWP TFTs show typical unipolar *p*-channel features, implying that the Fermi level of the channel in the AWP TFTs is difficult to be shifted upward to approach the vicinity of CBM, unable to make the *n*-channel inversion. The difficulty in shifting the Fermi level is generally related to the subgap DOS. The subgap DOS of the AWP, ABP, and AAP TFTs are examined using device simulation. We mainly considered the band tail states near the VBM, since SnO is an intrinsically *p*-type semiconductor. Detailed information about the simulation can be found in the Experimental Methods section and in the Supporting Information (Figure S1 and Table S1). Figure 4

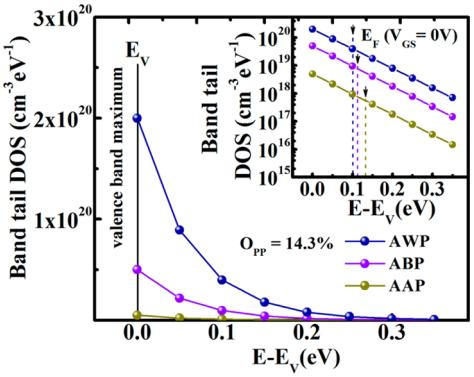

Figure 4. Band tail DOS for the AWP, ABP, and AAP TFTs estimated from device simulation and (inset) the plot with a logarithmic scale.

presents the band tail DOS of the active layers corresponding to the AWP, ABP, and AAP TFTs fabricated at O_{PP} = 14.3%. Specifically, the band tail DOS in the vicinity of the VBM for the channel layer in AWP, ABP, and AAP TFT is ~2.0×10^{20}, ~ 5.0×10^{19}, and ~5.0×10^{18} $cm^{-3}eV^{-1}$, respectively. Considering that the subgap states would decay exponentially from the VBM to the midgap, we estimated the total density of the trapped holes (N_T) as the Fermi level is lifted from V_{GS} = 0 V to the midgap. The Fermi level is calculated from the hole concentration (N_H) in the channel using the formula $N_H = N_V \exp[-(E_F - E_V)/k_BT]$,[24] where N_V is the effective density of states for the valence band (7.4×10^{19} cm^{-3}),[24] and k_B the Boltzmann constant. The estimated N_T is up to 2.6×10^{18} cm^{-3} in the AWP TFT, which is 2 orders of magnitude higher than that in a-IGZO TFTs.[25,26] This means that a very large gate voltage, about 49.1 V (roughly estimated by the relation $V_{GS} = N_T\, d/C$, where d is the thickness of the SnO active layer, and C is the capacitance of the SiO_2 layer), is necessary to deplete the holes so as to shift the Fermi level up to the midgap in the AWP TFT. This estimated value is roughly consistent with the V_{ON} value (45.6 V) obtained from the transfer curve. Nevertheless, the estimated N_T is decreased to ~5.9×10^{17} and ~5.9×10^{16} cm^{-3} for the ABP and AAP TFTs, respectively, in sharp contrast to that in the corresponding AWP devices. On basis of the experimental observation and device simulation, one can conclude that the unavailable ambipolar operation in the AWP TFTs is essentially due to the absence of minority carrier accumulation. This is attributed to the realistic difficulty in shifting the Fermi level freely caused by the present of tremendous subgap defect states. To realize ambipolar operation, one has to alleviate the subgap DOS in the SnO channel through material optimization, processing improvement such as surface passivation, or both. Based on Figure 1h, it was proved that the so-called AAP processing was successful to obtain ambipolar operation. In the following section, we will focus on understanding the role of the passivation layer.

The Role of the Passivation Layer. In the bottom-gate SnO TFTs, passivation on the back-channel surface is important whether for shielding the environmental exposure or for electrical stability. We will discuss the latter case in detail in the following section. For the former case, the passivation layer can shield the active layer from the surrounding

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atmosphere such as O_2 or H_2O molecular in air.[4] However, the operation conversion from *p*-type to ambipolar is not directly coupled with the shielding effect of the passivation layer. First, with changing the thickness of Al_2O_3 passivation layer in the AAP TFTs, it was found that V_{ON}, on/off current ratio, and μ_{FE} of them exhibit marginal variations (Supporting Information, Figure S2). Second, to examine the influence of environmental active gas such as O_2 or H_2O, another group of SnO TFTs (the active layers were deposited at O_{PP} = 14.3%) were annealed in vacuum (<1 × 10^{-4} Pa) instead of in air. The preadsorbed O_2 and H_2O molecules on the SnO back-channel surface can be pumped out,[4] so the influence of them on the SnO active layer is reduced to the minimum. It is interesting to see that the vacuum-annealed TFTs demonstrate almost the same variation tread as the air-annealed ones (Supporting Information, Figure S3). For example, the vacuum-annealed AAP TFTs displays a V-shaped transfer curve with V_{ON} = 15.4 V, and the ambipolar operation features can also be verified by the output characteristics.

Another passivation effect is the so-called chemical passivation, through which the surface defect states of semiconductor layer can be reduced significantly by eliminating the dangling bonds by, a thin dielectric layer. For example, the midgap interface defect density of c-Si can be as low as ~1 × 10^9 $eV^{-1}cm^{-2}$ after the introduction of a thermal SiO_2 film and a subsequent annealing.[27] The AAP processing in this study is analogous to this approach. Moreover, on one side, it is well-known that the nanocrystalline or amorphous oxide semiconductors are rich of the structural disorder, various defects (vacancies, interstices, substitutions, impurities, grain boundaries, and surface dangling bonds, etc.), or both, yielding abundant band tail and midgap states;[28] on the other, the surface and interface, with respect to the bulk, would contribute to the overall device properties more and more importantly as the surface-to-volume ratio is higher for the ultrathin film-stacked heterostructure. In view of both the nanocrystline nature and ultrathin (20 nm) SnO stacked device structure in our case, it is reasonably speculated that back-channel surface passivation in conjunction with appropriate annealing treatment would alleviate the subgap DOS, promoting Fermi level shift from near VBM toward CBM to trigger *n*-channel inversion.

The suppression of surface defect states through the passivation process can be monitored by the variation of the subthreshold voltage swing (S):[29]

$$S = \frac{kT}{q\log(e)}\left[1 + \frac{q}{C_i}\left(\sqrt{\varepsilon_s\left(N_{bulk}^{in} + N_{bulk}^{sur}\right)} + qN_{int}\right)\right] \quad (1)$$

where k is the Boltzmann constant, T the absolute temperature, q the electron charge, C_i the capacitance of the gate dielectric, ε_s the dielectric constant of semiconductor, and N_{int} the trap state density at the SiO_2/SnO interface. The bulk trap state density of the SnO channel is divided into internal trap state density N_{bulk}^{in} and trap state density near the back-channel surface N_{bulk}^{sur} (a few nanometers in thickness), as shown in Figure 5a. Figure 5b presents the variation of S as a function of O_{PP}. The subthreshold voltage swing at each O_{PP} decreases in order of AWP, ABP, and AAP, in line with the variation of the band tail DOS in the vicinity of the VBM, as shown in Figure 4. It should be noted that the fabrication processes of the AWP and ABP TFTs were kept the same, except that the latter one was covered by a passivation layer on the back-channel surface. It is believed that the deposition of a passivation layer could not bring about any changes in the microstructure and chemical bonding states of the SnO channel layer, as supported by the X-ray diffraction (XRD) and XPS results (Supporting Information, Figure S4), respectively. Therefore, the N_{int} and N_{bulk}^{in} in eq 1 for the AWP TFTs are considered as the same as those for the ABP TFTs, implying that the smaller S for the ABP TFTs is mainly resulted from smaller N_{bulk}^{sur}. For the AAP TFTs, the crystallinity of SnO channel layer is similar to the other two, but the metallic Sn content in the matrix is a slightly higher (Supporting Information, Figure S4b), suggesting that the SnO channel deviates from stoichiometry. Generally, the more nonstoichiometry of a material, the more defect states inside it, that is, the higher N_{int} and N_{bulk}^{in}, which will be discussed in detail in the next section. Therefore, in comparison with the AWP and ABP TFTs, the sharp drop of S in the AAP TFTs is undoubtedly associated with a reduction of SnO back-channel surface trap states N_{bulk}^{sur}.

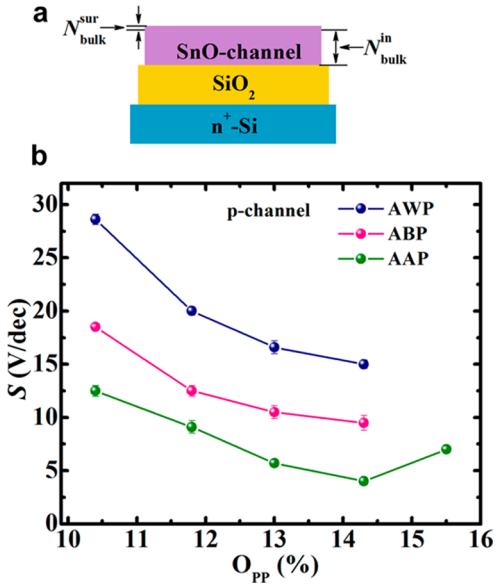

Figure 5. (a) Schematics of the distinction in the surface and internal bulk trap states in the SnO active layer. (b) The S values of the AWP, ABP, and AAP-processed TFTs as a function of O_{PP}.

In the ABP process, the surface states would be formed due to temperature-driven surface reconstruction, and the subsequent passivation process relieves a part of surface states. However, in the AAP process, the formation of surface states was suppressed effectively during annealing, because the surface of SnO channel layer has been passivated before annealing. The weak correlation between the key AAP TFT parameters and passivation layer thickness indicates that the channel surface passivation takes place at the SnO/Al_2O_3 interface, regardless of the passivation layer thickness, as evident in the Supporting Information (Figure S2). The passivation layer and appropriate processing sequence (AAP in this study) are capable of preventing the formation of surface defect states, yielding strong *n*-type inversion and ambipolar operation eventually.

Besides the Al_2O_3 passivation, we have also used SiO_2 as the passivation layer. The SiO_2 passivated SnO TFTs also demonstrate an operation mode conversion in order of AWP, ABP, and AAP process, similar to the Al_2O_3 passivated cases (Supporting Information, Figure S5). This again confirmed that the chemical passivation effect plays a very important role in the

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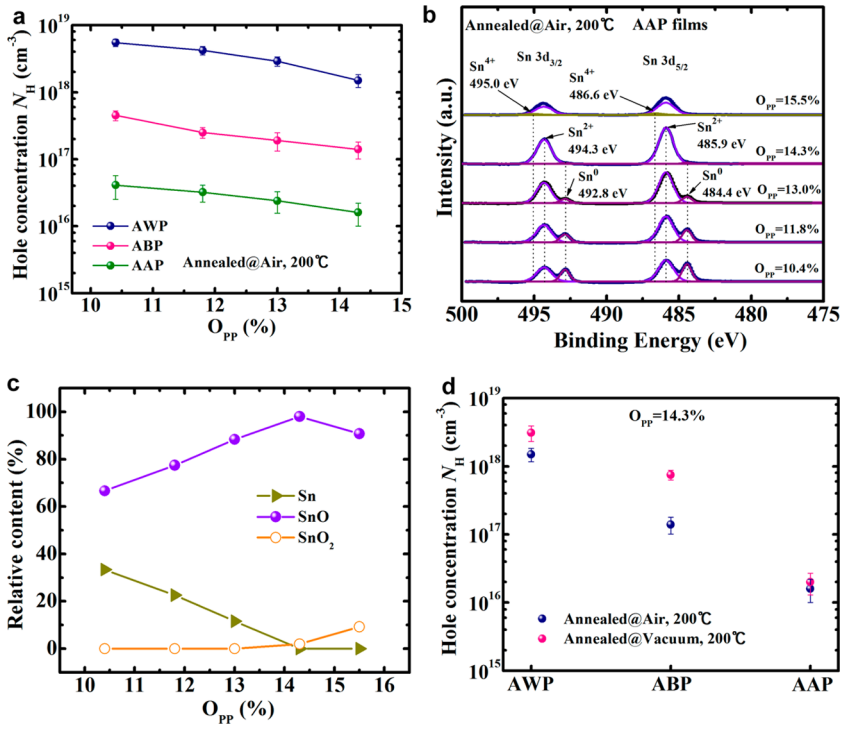

Figure 6. (a) The hole concentration of SnO films processed under AWP, ABP and AAP condition as a function of O_{PP}. (b and c) Core-level photoelectron spectra of Sn 3d and relative content of metallic Sn, SnO, and SnO_2 in the AAP-processed SnO films as a function of O_{PP}. (d) Comparison of hole concentration between the air-annealed and vacuum-annealed SnO films that were both deposited at O_{PP} = 14.3%.

operation mode conversion of SnO TFTs. In our previous report,[16] the SnO TFTs fabricated by electron-beam evaporation without passivation did show ambipolar features as well, with the *p*- and *n*-channel mobilities a little bit smaller than the optimal values in this article. It is believed that different deposition method and different nature of the fabricated channel material could account for that.

Hole Concentration Variation in the Sn-Rich SnO. The first-principle calculations suggested that the O-rich SnO is favorable for hole generation because the formation energy of the native acceptor defect (i.e., Sn vacancy) in the O-rich condition is lower than that in the Sn-rich condition.[9] However, our experimental results are opposite to this theoretical prediction. We systematically studied the influence of the O_{PP} on the hole concentration of SnO films under the AWP, ABP, and AAP processing condition using Al_2O_3 as the passivation layer. As illustrated in Figure 6a, the hole concentration of the AWP, ABP, and AAP processed SnO films all decrease as the O_{PP} increases, in line with the negative-shift of V_{ON} in the corresponding TFTs. In particular, the hole concentration of the AWP- and AAP-processed SnO films is above 1×10^{18} cm^{-3} and below 1×10^{17} cm^{-3} at each O_{PP}, respectively; while that of the ABP-processed films are in-between. The hole concentration at O_{PP} = 15.5% is not available due to the high resistance of the films. XPS measurements were used to investigate the chemical bonding states in the SnO matrix, and AAP-processed films were selected as the representatives, as shown in Figure 6b,c. When O_{PP} > 14.3%, excess oxygen induces the formation of Sn^{4+}, and the introduction of Sn^{4+} in the SnO matrix augments the disorder degree, giving rise to the high resistance of the film and the degradation of the TFT performance. When $O_{PP} \leq$ 14.3%, both metallic Sn and Sn^{2+} components are present in the films, and the content of metallic Sn decreases with increasing O_{PP}. In addition, it is observed that the hole concentration of the vacuum-annealed SnO films is higher than that of the air-annealed ones (Figure 6d), in accordance with the device performance (Supporting Information, Figure S3 vs. Figure 1). The vacuum-annealed films have more metallic Sn than the air-annealed ones. Overall, the variation of the hole concentration is in phase with that of the metallic Sn content, in accordance with previous reports.[20,30] This result suggested that metallic Sn-related defects, acting as acceptor states, can generate free holes in the metallic Sn-rich SnO films. However, further work is necessary to uncover why metallic Sn-related defects can act as acceptor states in Sn-rich SnO films. On the other hand, with decreasing O_{PP}, all the three kinds of TFTs show gradual degradation of *S*, on/off current ratio, and μ_{FE} in the *p*- and *n*-channel operations (Figures 2 and 5b), which is also suggested to be related to the increasing metallic Sn content. In oxide TFTs, it is believed that far from stoichiometry would lead to more defect states (including N_{int} and N_{bulk}^{in}).

It should be noted that the hole concentration at each O_{PP} was decreased in order of AWP, ABP, and AAP (Figure 6a), but the content of metallic Sn in the AAP processed films was the highest (Supporting Information, Figure S4b), which is opposite to the conclusion presented above. This contradiction indicates that another mechanism should dominate over the influence of the chemical bonding states, which is also considered to be the chemical passivation effect of the surface states as analyzed in The Role of the Passivation Layer. Concerning the relationship between the carrier concentration and field-effect inversion, generally speaking, channel layers with high carrier concentration are commonly difficult to be depleted,[31] so the polarity-reversal is unavailable. With regard to our case, the channel layers of AAP-TFTs with moderately low hole concentration enable *n*-channel inversion and ambipolar operation.

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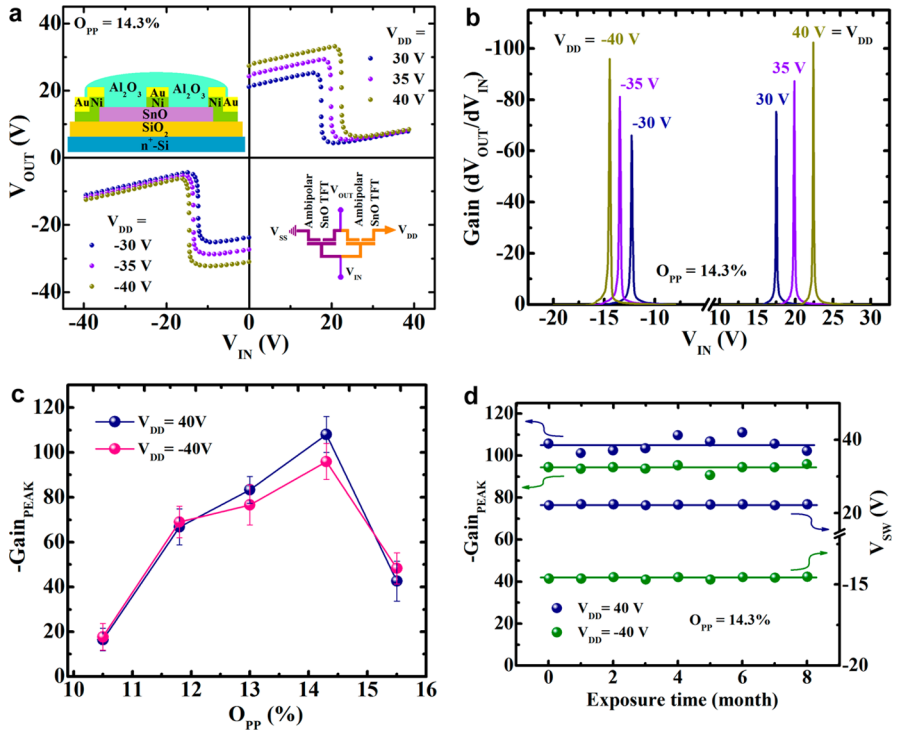

Figure 7. (a) Schematics of inverter structure (the second quadrant) and equivalent circuit (the fourth quadrant), and typical voltage transfer characteristics of CMOS-like inverters in which the channel layers were deposited at O_{PP} = 14.3%. Depending on the polarity of the V_{DD}, the inverters operate in the first quadrant or third quadrant. (b) Variations of the voltage gains of the inverters with V_{IN} at various V_{DD}, in which the channel layers were deposited at O_{PP} = 14.3%. (c) Dependence of the peak gains of the ambipolar inverters on O_{PP} at V_{DD} = ± 40 V. (d) Variations of the peak gains and the V_{SW} with exposure duration in air at V_{DD} = ± 40 V for the ambipolar inverters, in which the channel layers were deposited at O_{PP} = 14.3%.

Ambipolar SnO Inverters. The CMOS-like inverters were constructed by connecting two identical ambipolar TFTs, which are fabricated under the AAP processing condition using Al_2O_3 as the passivation layer. The schematics of the inverter structure and equivalent circuit are exhibited in Figure 7a, in which the voltage transfer characteristics (VTCs) of the ambipolar inverters with the SnO channel layer deposited at O_{PP} = 14.3% (Figure 1h,i) are also presented. The supply voltages (V_{DD}) are ±30, ± 35, and ±40 V in the first quadrant (positive V_{DD} and positive V_{IN}) and the third quadrant (negative V_{DD} and negative V_{IN}), respectively. Depending on the polarity of V_{DD}, distinct voltage switch behavior is observed in both the first and third quadrants. The voltage gain, defined as dV_{OUT}/dV_{IN}, is shown in Figure 7b. The peak gains are 75.3, 87.2, and 102.3 corresponding to V_{DD} = 30, 35, and 40 V in the first quadrant, and 66.0, 81.1, and 95.9 corresponding to V_{DD} = −30, −35, and −40 V in the third quadrant, respectively. The noise margin, as another key parameter for an inverter, reflects the stability of the V_{OUT} to the signal interference. Noise margins at high input level (NM_H) and low input level (NM_L) are defined by $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$, where V_{OH}, V_{OL}, V_{IH}, and V_{IL} are output and input voltage at high and low levels, respectively, which are determined by V_{IN} in that $|dV_{OUT}/dV_{IN}| = 1$. The NM_H and NM_L are estimated to be 9.2 and 14.1 V for V_{DD} = 40, 7.3, and 14.9 V for V_{DD} = −40 V, respectively. High voltage gains and wide noise margins are obtained simultaneously. Figure 7c exhibits the peak gains as a function of O_{PP}. At V_{DD} = 40 V, the peak gains increase from 16.5 to 102.3 as O_{PP} increases from 10.4 to 14.3%, then decrease to 42.6 as O_{PP} further increases to 15.5%. The same variation trend of the peak gains are also observed at V_{DD} = −40 V. Basically, the dependence of the inverter voltage gain on O_{PP} is related to the mobility, on/off current ratio, and symmetric output characteristics of the ambipolar transistors, etc. The voltage gain recorded in this paper is competitive in comparison with the previous reports.[15,16,23,32−34] The device stability was checked in terms of the voltage gain and switching threshold voltage V_{SW} (at $V_{IN} = V_{OUT}$) as a function of air exposure duration, and the results are presented in Figure 7d. After being exposed in air over eight months, the inverters nearly did not show any degeneration in the voltage gain and the threshold voltage. The long-term device reliability and stability are achieved owing to the back-channel surface passivation, through which the interaction between the semiconductor channel layer and external environment is precluded.

CONCLUSIONS

We have demonstrated that ambipolar SnO TFTs can be utilized as the building blocks to design and construct compact CMOS-like logic devices and circuits. The operation mode conversion from *p*-type to ambipolar and device stability are obtained simultaneously by introducing a passivation layer onto the back-channel surface. The chemical passivation effect would reduce back-channel surface states, leading to a cascade effect, that the subgap states are getting suppressed. Therefore, the Fermi level of SnO channel can be shifted freely between the valence band and conduction band upon the gate voltage magnitude and polarity, resulting in both the *p*- and *n*-channel operation. By means of in situ tuning O_{PP} during channel layer deposition, in conjunction with appropriate passivation sequence and annealing treatment, the performance of

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ambipolar SnO TFTs can be systematically modified and eventually optimized. CMOS-like inverters based on ambipolar SnO TFTs are constructed successfully, featuring simplified circuit design and fabrication processes. Large inverter voltage gains (>100) along with wide noise margins are achieved based on the optimization of the channel layer properties and ambipolar transistor performance. This demonstration allows further development of low-cost and large-area oxide-based CMOS-like circuits, with a decreased number of device components. For future development, it is proposed that we should pay more attention to the anisotropic transporting properties of SnO in order to boost its mobility and pave the way for high-speed electronic applications, because SnO has a layered structure with a loosely bonded van der Waals gap.

■ ASSOCIATED CONTENT

Supporting Information

Additional details on the device simulation, influence of the Al_2O_3 layer thickness on the performance of the ambipolar SnO TFTs, electrical properties of vacuum-annealed SnO TFTs, microstructures and chemical bonding states of SnO films, and transfer and output characteristics of SiO_2 passivated SnO TFTs. The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.5b02964.

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Notes

The authors declare no competing financial interest.

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