IOPscience iopscience.iop.org

Home Search Collections Journals About Contact us My IOPscience

Anomalous bias-stress-induced unstable phenomena of InZnO thin-film transistors using Ta_2O_5 gate dielectric

This article has been downloaded from IOPscience. Please scroll down to see the full text article.

2012 J. Phys. D: Appl. Phys. 45 205103

(http://iopscience.iop.org/0022-3727/45/20/205103)

View the table of contents for this issue, or go to the journal homepage for more

Download details:
IP Address: 210.72.19.250
The article was downloaded on 02/05/2012 at 03:21

Please note that terms and conditions apply.

IOP PUBLISHING JOURNAL OF PHYSICS D: APPLIED PHYSICS

J. Phys. D: Appl. Phys. **45** (2012) 205103 (5pp) doi:10.1088/0022-3727/45/20/205103

Anomalous bias-stress-induced unstable phenomena of InZnO thin-film transistors using Ta_2O_5 gate dielectric

Wangying Xu, Mingzhi Dai, Lingyan Liang, Zhimin Liu, Xilian Sun, Qing Wan and Hongtao Cao

Ningbo Institute of Materials Technology and Engineering (NIMTE), Chinese Academy of Sciences (CAS), Ningbo 315201, People's Republic of China

E-mail: h_cao@nimte.ac.cn

Received 4 January 2012, in final form 20 February 2012
Published 1 May 2012
Online at stacks.iop.org/JPhysD/45/205103

Abstract

InZnO thin-film transistors using high-κ Ta_2O_5 gate dielectric are presented and analysed. The large capacitance coupling effect of amorphous Ta_2O_5 results in fabricated devices with good electrical properties. However, an anomalous negative threshold voltage (V_{th}) shift under positive bias stress is observed. It is suggested that electron detrapping from the high-κ Ta_2O_5 dielectric to the gate electrode is responsible for this V_{th} shift, which is supported both by the logarithmical dependence of the V_{th} change on the duration of the bias stress and device simulation extracted trapped charges involved.

(Some figures may appear in colour only in the online journal)

1. Introduction

Amorphous oxide thin-film transistors (TFTs) have attracted ever-increasing attention as backbone electronics for active-matrix liquid crystal displays (AMLCDs) and active-matrix organic light-emitting diode displays (AMOLEDs). This is mainly due to the advantages of amorphous oxide semiconductors, such as visible light transparency, high carrier mobility and large-area uniformity even when fabricated at low temperatures [1–3]. Recently, considerable effort has been devoted to realizing low power consumption for flexible, mobile and battery-powered applications using oxide-based TFTs with high-κ gate dielectrics. In general, the high-κ dielectrics in TFTs play an important role in decreasing the subthreshold slope and operating voltage owing to their huge capacitive coupling between the gate and active layer. A few promising results have been reported using high-κ gate dielectrics for oxide-based TFTs [4–10]. However, it is still necessary to investigate the deposition method, leakage current behaviour, trap states in the dielectric bulk and the related device instability in the high-κ/amorphous oxide-based TFTs. The electrical stability of the TFT is especially pivotal in the case of current-driven OLED displays because it would change the brightness of an individual pixel and cause display nonuniformity [3].

In this study, we report on the use of a high-κ, amorphous Ta_2O_5 gate dielectric to produce InZnO-based TFTs. Then the electrical dynamics of the devices under positive bias stress and their recovery behaviour were investigated. In order to clarify the degradation mechanism, TFT device simulations [11, 12] were also performed. It is revealed that electron detrapping from the high-κ Ta_2O_5 to the gate electrode is responsible for the unusual sweep hysteresis and threshold voltage shift under positive bias stress.

2. Experiment details

The fabricated TFTs have a bottom gate and top contact configuration. First, a 125 nm Ta_2O_5 gate dielectric layer was deposited on a cleaned indium tin oxide (ITO) glass substrate by radio frequency (rf) magnetron sputtering at room temperature. The deposition conditions were as follows: input power of 80 W, total sputtering pressure of 0.27 Pa, gas mixing ratio of $Ar/O_2 = 5/1$ and substrate bias of 60 V. Next, a 50 nm InZnO channel layer was deposited through a shadow mask by rf magnetron sputtering. The deposition process of the InZnO film was described elsewhere [10]. Then, Ti (80 nm) and Au (50 nm) were sequentially e-beam-evaporated through another shadow mask to form the source and drain electrodes. Finally, the TFTs were annealed at 200 °C in air for 1 h. The

0022-3727/12/205103+05$33.00 © 2012 IOP Publishing Ltd Printed in the UK & the USA

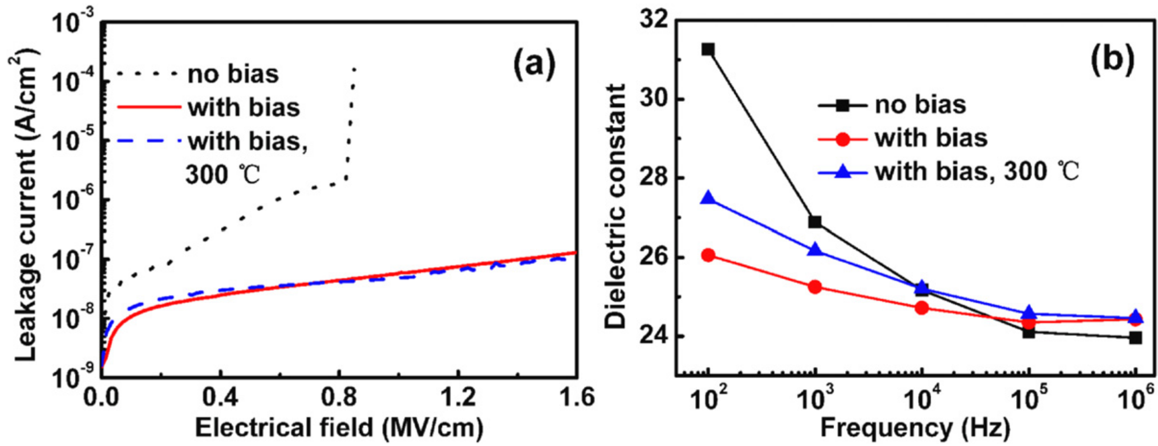

Figure 1. (*a*) Leakage current of the Ta_2O_5 films without substrate bias, with substrate bias, and annealed at 300 °C (the biased one). (*b*) Dielectric constant of the same films as a function of frequency.

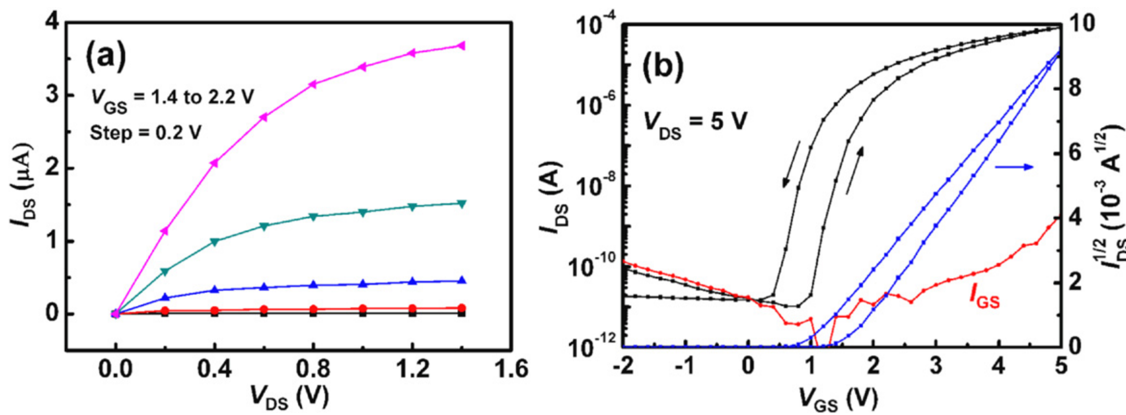

Figure 2. (*a*) Output characteristics and (*b*) transfer characteristics of the InZnO TFT with Ta_2O_5 gate dielectric.

devices had a channel length (L) and width (W) of 100 μm and 500 μm, respectively. The ITO/Ta_2O_5/Cu capacitors were also fabricated to characterize the capacitance and leakage current of the Ta_2O_5 insulators. The electrical characteristics of the devices were measured with a precision semiconductor analyser (Keithley 4200) in the dark at room temperature.

3. Results and discussion

Figure 1 shows the leakage current and the dielectric constant frequency dispersion nature of the Ta_2O_5 films with or without substrate bias during sputtering. All the Ta_2O_5 films were amorphous in nature deduced from x-ray diffraction measurements. Generally, an amorphous structure is preferred because grain boundaries may act as preferential paths for impurity diffusion and leakage current in the polycrystalline dielectrics. In addition to that, amorphous materials present flat surfaces, giving rise to superior dielectric/semiconductor interfacial properties [4]. The film prepared by bias-assisted sputtering has a much lower leakage current ($\sim 10^{-7}$ A cm^{-2} at 1.6 MV cm^{-1}) as well as much weaker frequency dispersion of the dielectric constant, indicating that a much lower defect concentration is present in the film [8]. Generally, proper ion-bombardment conditions (through substrate bias) favour the growth of more densely packed films. The increase in density is believed to be a result of the beneficial 'soft-hammering' effect of ion bombardment, which can contribute to increasing the mobility of the adatoms arriving at the surface of the film. The increase in the film density is naturally accompanied by a decrease in the density of pores and/or microvoids in the film, thereby reducing the absorption of moisture and other gaseous contaminants in the film. The electrical performance can be improved resultantly with the film densification caused by substrate bias [13]. Moreover, the structure and electrical characteristics of the Ta_2O_5 film remain almost unchanged after annealing at 300 °C (figure 1). Therefore, it is proposed that substrate bias assisted sputtering is an effective method to fabricate Ta_2O_5 films with low leakage current, which is desirable for the fabrication of oxide-based TFTs featuring low thermal budget.

Figures 2(*a*) and (*b*) illustrate the output and transfer characteristics of InZnO/Ta_2O_5 TFTs. The devices exhibited a large saturation mobility (μ_{sat}) value of 17 cm^2 V^{-1} s^{-1}, an excellent subthreshold slope (S) of 140 mV/decade, a low threshold voltage (V_{th}) of 1.6 V and a high on–off current ratio (I_{on}/I_{off}) up to 10^7. Even if the quality of the sputtered Ta_2O_5 is far from optimal, the tremendous capacitance provided by the high-κ dielectric can result in small S and V_{th}. To evaluate the initial stability of the TFTs with high-κ dielectric, electrical measurements were performed in double sweep mode to study

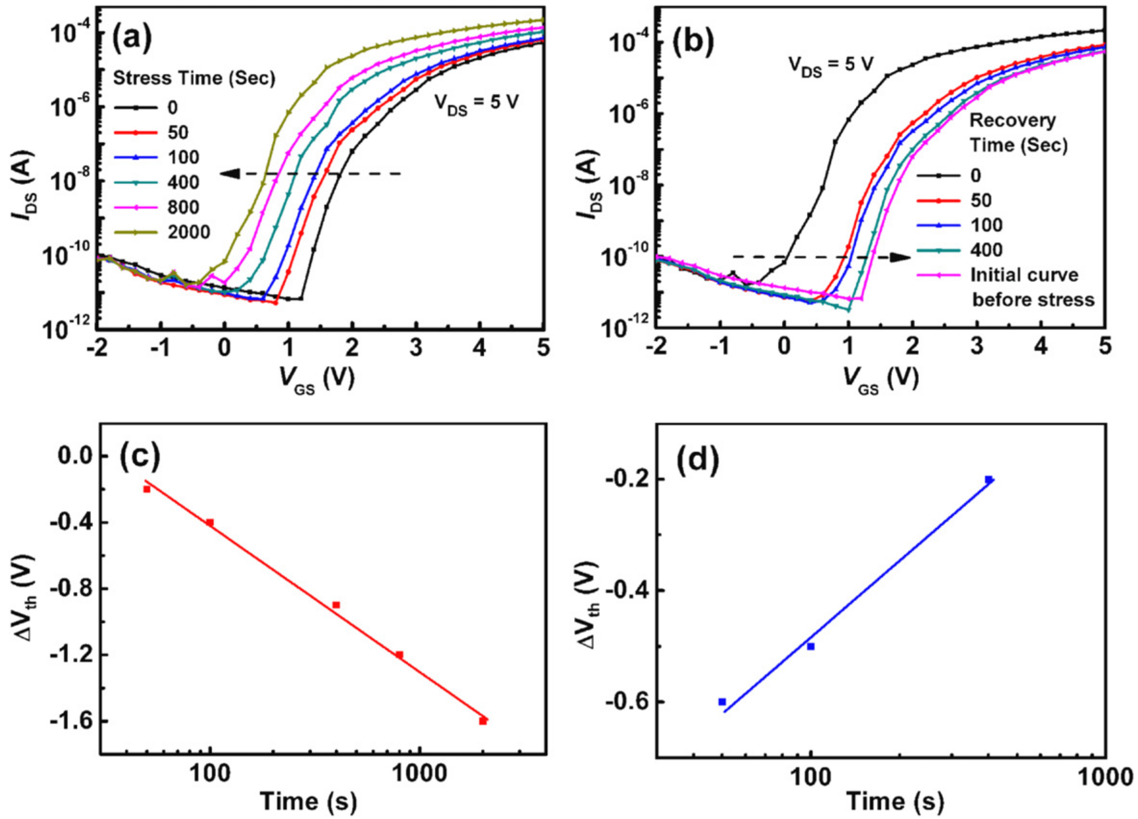

Figure 3. (*a*) Transfer characteristics of the InZnO TFT with Ta_2O_5 gate dielectric as a function of stress time. (*b*) Transfer characteristics as a function of recovery time after stress. (*c*) Time dependence of ΔV_{th} during the stress phase. (*d*) Time dependence of ΔV_{th} during the recovery phase.

the hysteresis of the devices. Interestingly, an anomalous counterclockwise hysteresis accompanied by a V_{th} shift of −0.6 V was observed, which is worth studying in more detail.

The evolution of transfer curves for the Ta_2O_5-gated devices under bias stress is presented in figures 3(*a*) and (*b*). The device was stressed with a positive gate bias of 3 V and V_{DS} of 5 V. The maximum stress duration was 2000 s, and afterwards the bias was switched to the ground, in order to observe the recovery behaviour. The variations of V_{th} (ΔV_{th}) with the time during stress and recovery phases are depicted in figures 3(*c*) and (*d*). Basically, under a positive bias stress, oxide-based TFTs using thermally grown SiO_2 or PECVD made SiO_x/SiN_x gate dielectrics always show positive V_{th} shifts, which is due to electron trapping in the gate dielectric or/and at the channel/dielectric interface [14–16]. However, our Ta_2O_5-gated devices produced an anomalous negative V_{th} shift when subjected to a positive bias stress. This anomalous shift is in accordance with the aforementioned counterclockwise hysteresis displayed in figure 2(*b*) [14]. Note that SiO_2-gated InZnO TFTs exhibit normal positive V_{th} shift, so this unusual V_{th} shift cannot be caused by the channel layer exclusively.

Although the precise origin is unclear, there are several possible reasons for this bias-stress-induced instability in the InZnO TFTs using Ta_2O_5 gate dielectric: (1) slow polarization of the gate dielectric [17]; (2) ion migration within the gate dielectric [14]; (3) charge trapping/detrapping in the gate dielectric [3, 18, 19]. Firstly, the possibility of slow polarization in the gate dielectric can be excluded, because slow polarization is usually observed in dielectrics containing polar groups that slowly move/reorient in the external electric fields, such as in polymers having polar side groups [17]. Secondly, both positive and negative ion migration within the insulator can give rise to a negative V_{th} shift, which is in line with our experimental results (figure 3(*a*)). However, our devices show fast recovery of V_{th} when relaxed without the annealing treatment (figure 3(*b*)). If ion drift were the dominant instability mechanism, retesting after an extended period of rest time would be 'irreversible' since there is no driving force for ions to diffuse back to their original locations [14]. As a result, the present V_{th} shift is reasonably attributed to the charge trapping/detrapping in the gate dielectric.

As depicted in figure 3(*a*), the Ta_2O_5-gated TFTs exhibited a negative V_{th} shift without a significant change in the *S* value when subjected to a positive bias stress. Moreover, the device produced very fast recovery, leading to a decrease in ΔV_{th} down to −0.2 V after only 400 s relaxation without any annealing (figure 3(*b*)). These suggest that charge trapping/detrapping is the dominant mechanism to account for the stability issue of the Ta_2O_5-gated devices [14, 18]. The investigation on the time dependence of ΔV_{th} can be used to confirm the dominant mechanism causing the bias-stress-induced V_{th} shift in TFTs [20]. The V_{th} shift is linearly proportional to the logarithmic time, as observed both in figures 3(*c*) and (*d*), indicating that charge trapping/detrapping is the dominant mechanism in the Ta_2O_5 devices. The

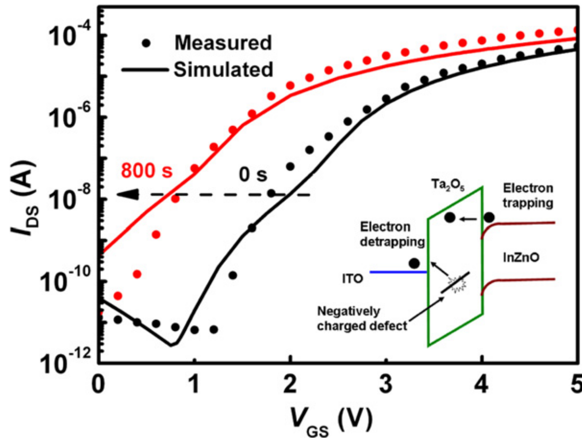

Figure 4. Measured (symbols) and simulated (lines) transfer curves for InZnO TFTs with Ta_2O_5 gate dielectric before and after bias stress for 800 s. The inset shows the schematic diagram of the Ta_2O_5 device when subjected to a positive bias stress.

logarithmic dependence of ΔV_{th} on time is defined as

$$\Delta V_{th} = r_0 \log\left(\frac{t}{t_0}\right),$$

where r_0 is a decay rate constant which is related to the density of traps in the dielectric and the tunnelling constant [21, 22].

There are two candidate mechanisms for this negative V_{th} shift when subjected to a positive bias stress. One is hole trapping in the high-κ dielectric, and the other is electron detrapping from the high-κ dielectric [19]. However, it is hard to believe that holes can be generated in this n-channel device without light illumination [23]. Moreover, under positive stress, hole trapping in the high-κ dielectric is restrained. Therefore, it is suggested that this negative V_{th} shift is not ascribed to hole trapping but electron detrapping from the high-κ Ta_2O_5 dielectric. To further confirm this proposed mechanism, TFT device simulations were performed. Figure 4 presents the measured (symbols) and simulated (lines) transfer curves of the Ta_2O_5-gated device before and after 800 s bias stress. After bias stress, the simulated curve can fit well with the experimental one just by adjusting the trapped charge (Q) without change in the other parameters [24]. Q is the combination effects of the dielectric bulk trap states and the channel/dielectric interfacial trap states, which can be extracted based on the simulation [21, 24]. The values of Q are -1.5×10^{12} cm^{-2} and -3×10^{11} cm^{-2} for the initial device and the device after bias stress, respectively. The decrease in Q might be due to electron detrapping from the dielectric. In comparison with the experimental value of $\Delta Q = C_{Ta_2O_5}(V_{th}^{800\,s} - V_{th}^{0\,s}) = -1.3 \times 10^{12}$ cm^{-2}, the values of simulated Q are believed to be reasonable. As illustrated in figure 4 (inset), electron detrapping from the Ta_2O_5 dielectric to the ITO gate dominates over electron trapping in the gate dielectric or/and at the channel/dielectric interface, leading to this anomalous negative V_{th} shift.

Note that a high-κ material fabricated by magnetron sputtering often contains high density of defect states, so electron detrapping from negatively charged defect is likely to occur under positive bias stress [4, 9, 19]. At present, experiments are in progress to clarify the nature of charge defect states in Ta_2O_5 dielectric responsible for the unusual V_{th} shift in this case, which favours uncovering the restrictive element to get rid of the negatively charged defects present in the Ta_2O_5 films and to find a method to optimize the sputtering deposition procedure, since our dielectric deposition condition is far from optimal so far. This implementation could be achieved by optimizing the substrate bias, input power, low-temperature *in situ* heating and gas mixing ratio of Ar/O_2 during sputtering. Alternatively, ALD deposition technology can be used to fabricate Ta_2O_5 films approaching stoichiometry for practical use. Moreover, standard photolithography and etching processes must be introduced to realize shorter/narrower devices and further reduce the gate leakage current [17].

4. Conclusions

In summary, we have demonstrated InZnO TFTs using high-κ Ta_2O_5 dielectric grown by substrate bias assisted magnetron sputtering. Due to the defect-free grain boundary and surface flatness of the amorphous structure of Ta_2O_5, TFTs show a large μ_{sat} of 17 cm^2 V^{-1} s^{-1}, a small S of 140 mV/decade, a low V_{th} of 1.6 V and a high I_{on}/I_{off} of 10^7. An anomalous negative V_{th} shift was observed for the Ta_2O_5 TFTs when subjected to a positive bias stress, which is ascribed to the electron detrapping from the high-κ Ta_2O_5 dielectric to the ITO gate electrode, as manifested by the logarithmical dependence of the V_{th} change on the duration of the bias stress as well as the decreased trapped charges extracted from the device simulation after bias stress exertion. Although high-κ dielectrics are effective in decreasing the subthreshold slope and operating voltage, better understanding of the physics and further optimizing the deposition method of high-κ materials in oxide-based TFTs are definitely indispensible for their real applications.

Acknowledgments

This work is supported by the Chinese National Program on Key Basic Research Project (2012CB933003), the National Natural Science Foundation of China (Grant No 11104289), the Science and Technology Innovative Research Team of Ningbo Municipality (2009B21005) and the Key Program for Science and Technology Innovative Team of Zhejiang Province (2010R50020).

References

[1] Park J C, Kim S, Kim S, Kim C, Song I, Park Y, Jung U I, Kim D H and Lee J S 2010 *Adv. Mater.* **22** 5512
[2] Barquinha P, Pereira L, Goncalves G, Martins R and Fortunato E 2009 *J. Electrochem. Soc.* **156** H161
[3] Lee J, Park J S, Pyo Y S, Lee D B, Kim E H, Stryakhilev D, Kim T W, Jin D U and Mo Y G 2009 *Appl. Phys. Lett.* **95** 123502
[4] Barquinha P, Pereira L, Gonçalves G, Martins R, Kuščer D, Kosec M and Fortunato E 2009 *J. Electrochem. Soc.* **156** H824

[5] Zhang L, Li J, Zhang X W, Jiang X Y and Zhang Z L 2009 *Appl. Phys. Lett.* **95** 072112
[6] Su N C, Wang S J and Chin A 2009 *IEEE Electron Device Lett.* **30** 1317
[7] Park J S, Jeong J K, Mo Y G and Kim S 2009 *Appl. Phys. Lett.* **94** 042105
[8] Kim J B, Fuentes-Hernandez C and Kippelen B 2008 *Appl. Phys. Lett.* **93** 242111
[9] Oh M S, Lee K, Song J H, Lee B H, Sung M M, Hwang D K and Im S 2008 *J. Electrochem. Soc.* **155** H1009
[10] Chen A H, Liang L Y, Zhang H Z, Liu Z M, Ye X J, Yu Z and Cao H T 2011 *Electrochem. Solid-State Lett.* **14** H88
[11] Hsieh H H, Kamiya T, Nomura K, Hosono H and Wu C C 2008 *Appl. Phys. Lett.* **92** 133503
[12] Fung T C, Chuang C S, Chen C, Abe K, Cottle R, Townsend M, Kumomi H and Kanicki J 2009 *J. Appl. Phys.* **106** 084511
[13] Brassard D, El Khakani M A and Ouellet L 2007 *J. Appl. Phys.* **102** 034106
[14] Wager J F, Keszler D A and Presley R E 2008 *Transparent Electronics* 1st edn (New York: Springer) p 142
[15] Dey A, Allee D R and Clark L T 2011 *Solid-State Electron.* **62** 19
[16] Choi J H, Han U B, Lee K C, Lee J H, Kim J J, Cho I T, Lee J H and Heo Y W 2009 *J. Vac. Sci. Technol.* B **27** 622
[17] Liu J, Buchholz D B, Hennek J W, Chang R P H, Facchetti A and Marks T J 2010 *J. Am. Chem. Soc.* **132** 11934
[18] Vygranenko Y, Wang K and Nathan A 2007 *Appl. Phys. Lett.* **91** 263508
[19] Sato M, Kamiyama S, Matsuki T, Ishikawa D, Ono T, Morooka T, Yugami J, Ikeda K and Ohji Y 2010 *Japan. J. Appl. Phys.* **49** 04DC24
[20] Lee J M, Cho I T, Lee J H, Cheong W S, Hwang C S and Kwon H I 2009 *Appl. Phys. Lett.* **94** 222112
[21] Suresh A and Muth J F 2008 *Appl. Phys. Lett.* **92** 033502
[22] Fujii M, Yano H, Hatayama T, Uraoka Y, Fuyuki T, Jung J S and Kwon J Y 2008 *Japan. J. Appl. Phys.* **47** 6236
[23] Kwon J Y, Jung J S, Son K S, Lee K H, Park J S, Kim T S, Choi R, Jeong J K and Koo B 2010 *Appl. Phys. Lett.* **97** 183503
[24] Cho E N, Kang J H, Kim C E, Moon P and Yun I 2011 *IEEE Trans. Device Mater. Reliab.* **11** 112