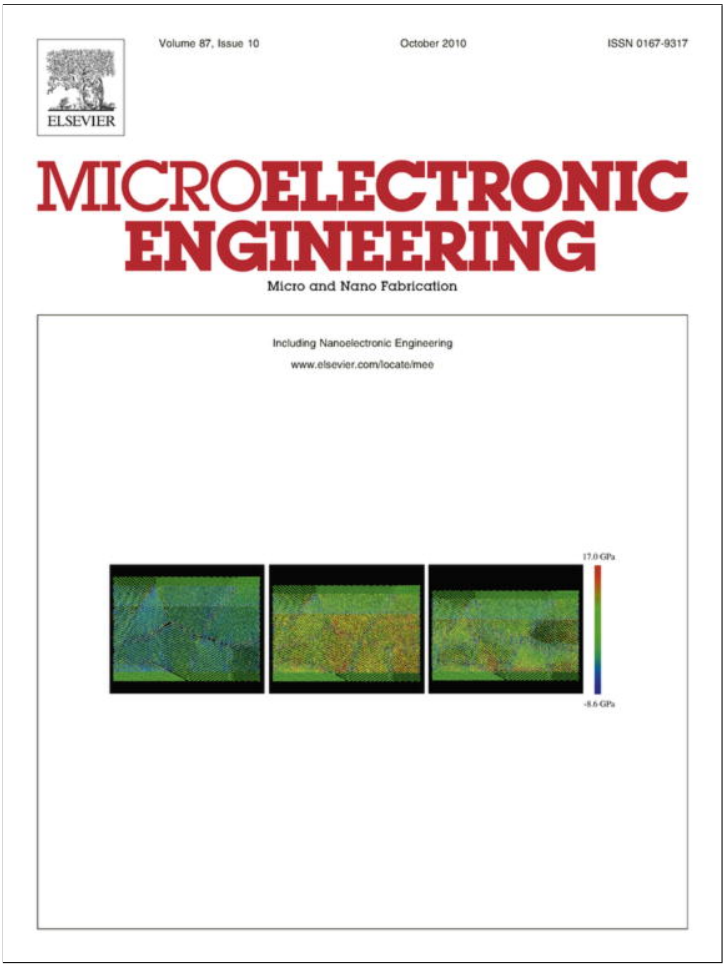

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Influence of the channel layer thickness on electrical properties of indium zinc oxide thin-film transistor

Ai Hua Chen [a], Hong Tao Cao [a,*], Hai Zhong Zhang [a], Ling Yan Liang [a], Zhi Min Liu [a], Zheng Yu [a], Qing Wan [a,b,*]

[a] Division of Functional Materials and Nano Devices, Ningbo Institute of Material Technology and Engineering, The Chinese Academy of Sciences, Ningbo 315201, People's Republic of China

[b] Key Laboratory for Micro-Nano Optoelectronic Devices of Ministry of Education, and State Key Laboratory of Chemo/Biosensing and Chemometrics, Hunan University, Changsha 410082, People's Republic of China

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ABSTRACT

Thin-film transistors (TFTs) were fabricated on SiO_2/n^+–Si substrates using amorphous binary In_2O_3–ZnO (a-IZO) films with different thickness for active channel layers deposited by the rf magnetron sputtering at room temperature. The performance of devices was found to be thickness dependent. With the active layer thickness from 33 to 114 nm, the field-effect mobility μ_{FE} increased from 1.60 to 4.59 cm^2/V s, the threshold voltage V_{TH} decreased from 62.26 to 20.82 V, and the subthreshold voltage swing S decreased from 4.06 V/decade to 1.30 V/decade. Further, the dependence of TFTs' electrical properties on active layer thickness was investigated in detail on the basis of free carrier density and interface scattering.

1. Introduction

Recently, transparent oxide semiconductors (TOSs) have been widely explored for their wide applications. Especially TOSs, such as ZnO [1,2], ZnMgO [3], Zn–Sn–O (ZTO) [4], SnO_2 [5], Ga_2O_3 [6], In–Ga–O (IGO) [7], In_2O_3 [8], In–Sn–O (ITO) [9], In–Ga–Zn–O [10,11] and so on, can be used as active channel layer for transparent thin-film transistors (TTFTs) with higher field-effect mobility compared with the conventional a-Si (amorphous Si) TFT. Among these oxides, IZO is one of potential candidates used as the active layer, because of its excellent optical transmission, high mobility, chemical stability, thermal stability, and smooth surface [12]. Moreover, all these properties are attainable even in amorphous phase, which implies IZO films could be deposited at room temperature for large area applications. Thus, a-IZO films allow for the development of inexpensive transparent and flexible electronic circuits [13].

Some previous work [14–16] reported that the channel layer thickness is one of vital factors affecting the performance of the TFT. In our study, a-IZO TFTs were fabricated with active layer thickness ranging from 33 to 114 nm in order to investigate the influence of active layer thickness on electrical properties of the TFTs.

2. Experimental

The a-IZO TFTs with a bottom gate structure were fabricated on a heavily-doped Si substrate with 300 nm thick SiO_2 formed via thermal oxidation. The schematic cross-sectional diagram of a-IZO TFT is illustrated in Fig. 1. The Si (the resistivity $\rho < 0.01\ \Omega$ cm) and the SiO_2 (capacitance per unit area $C_i = 10$ nF/cm^2) served as the substrate/gate electrode and the TFT gate dielectric, respectively. The SiO_2 surface was ultrasonically cleaned with acetone (5 min), ethanol (5 min), and deionized water (5 min) sequentially for two times. The a-IZO film was prepared by rf magnetron co-sputtering (ULVAC, Jsputter 8000) applying a 2 in. ZnO target (99.99%) at a power of 100 W and a 2 in. In_2O_3 target (99.99%) at 70 W. Prior to deposition, the chamber was evacuated to 1.70×10^{-4} Pa and each wafer was argon-plasma cleaned at 100 W at a pressure of 0.46 Pa for 3 min. The sputtering was carried out at room temperature and the working pressure for the film deposition was fixed at 0.46 Pa with Ar gas flow of 8 sccm and O_2 gas flow of 2 sccm. The distance between target and substrate was about 14.5 cm. The thickness of the a-IZO channel layer patterned by the first shadow mask varied from 33 to 114 nm by controlling the deposition time. After deposition of the a-IZO layer, 30 nm Ti/100 nm Au was deposited by electron beam evaporation (ULVAC MUE-ECO-EB) and the second shadow mask was used to form the source and drain electrodes. The a-IZO TFT channel was defined as the width $W = 500$ μm and the length $L = 100$ μm ($W/L = 5$). The first and second shadow masks were utilized to define the device

* Corresponding authors. Tel.: +86 574 86685161; fax: +86 574 86685163.
E-mail addresses: h_cao@nimte.ac.cn (H.T. Cao), Wangqing7686@hotmail.com (Q. Wan).

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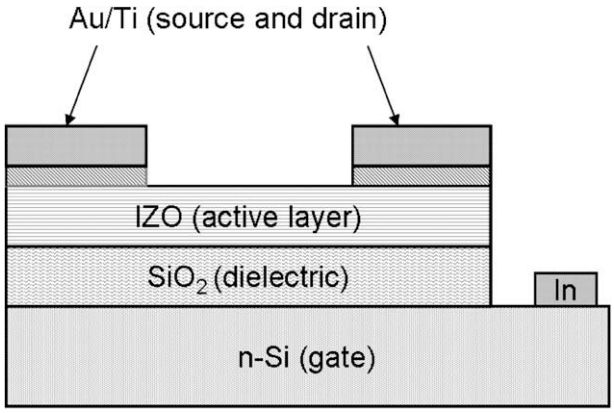

Fig. 1. Schematic cross-sectional diagram of the IZO-TFT structure fabricated at RT.

and source/drain pattern, respectively. Finally, all TFTs were treated by rapid thermal annealing (RTA) (RTP-500 V) at 300 °C for 5 min in air.

The thickness of a-IZO film was determined ex situ using spectroscopic ellipsometer (SE) (J.A. Woollam Co., Inc. M-2000DI). The active layer thickness of the TFTs was 33 nm, 61 nm, 88 nm, 114 nm, respectively. All the thickness results were double checked by a Surface Profiler (Alpha-Step IQ), in consistent with SE fitting results. The stoichiometry of the films was measured by EDX (EDAX, S-4800) on the RTA-treated wafer. X-ray diffraction (XRD, Bruker Discover) data was obtained by using Cu Kα radiation. The electrical characteristics of the TFTs were measured with a precision semiconductor analyzer (Keithley 4200) in dark at room temperature.

3. Results and discussion

Fig. 2 shows the XRD profile and spectra of refractive index of IZO films with different thickness. In Fig. 2A, only diffraction peaks of the substrate Si appeared at $2\theta = 25.71°$ and $2\theta = 28.47°$ in the XRD spectra. This indicates that both the as-deposited and RTA-treated IZO thin films are amorphous, which is in accord with Ref. [17]. The as-deposited IZO TFTs did not exhibit field-effect transistor characteristics, but the post-RTA-treated ones did. It is concluded that RTA process could improve the contact-resistance between Ti/Au electrode and the channel layer [18,19], and the local atomic arrangement of a-IZO layer that was not able to be detected by XRD. Additionally, the inset to Fig. 2A reveals a typical EDX pattern of post-RTA-treated 114 nm thick film and the stoichiometry (expressed as $(In_2O_3)_x{\cdot}(ZnO)_{1-x}$) of a-IZO films was found to be $x \sim 0.22$. The composition of other films is quite similar (not shown here). Fig. 2B shows refractive index of films obtained by fitting ellipsometric spectra examined via SE in the 450–900 nm spectral range. The dispersion model for SE data analysis is shown in the inset of Fig. 2B. It is discovered that the refractive index of a-IZO film augmented with the increase of thickness (d) in Fig. 2B. The refractive index is the indicator of the packing density of the films, so it is deduced that the packing density improves, as the thickness increases.

Fig. 3 reveals the output characteristics of the a-IZO TFTs with different channel layer thickness. In Fig. 3a and b, the gate–source voltage (V_{GS}) is increased from 0 to 80 V in steps of 10 V, and in Fig. 3c and d V_{GS} from 0 to 40 V in steps of 5 V. All devices exhibited nice pinch-off, high on-current and hard saturation characteristics with steep rise in the low drain–source voltage (V_{DS}), which is very desirable for practical applications of transistor. It is noted that the channel layer of the a-IZO TFT is n-type, as electron carriers are generated by the positive V_{GS} and all TFTs operate in enhancement mode.

Fig. 4 displays the typical transfer and $I_{DS}^{1/2} - V_{GS}$ characteristics of the devices, with small off-currents ($\sim 10^{-11}$ A), and good on/off-current ratios ($>10^{-6}$). The threshold voltage (V_{TH}) and field-effect mobility (μ_{FE}) in the saturation region of drain current were calculated based on the following equation:

$$I_{DS} = \frac{\mu_{FE} W C_i}{2L}(V_{GS} - V_{TH})^2 \quad \text{for} \quad V_{DS} > V_{GS} - V_{TH} \tag{1}$$

where C_i is the gate capacitance per unit area, W the channel width, L the channel length and I_{DS} the drain current. The subthreshold voltage swing (S) was determined by the following equation:

$$S = \frac{dV_{GS}}{d(\log I_{DS})} \tag{2}$$

As shown in Fig. 4, the field-effect mobility (μ_{FE}), threshold voltage (V_{TH}), subthreshold voltage swing (S), on/off ratio and off-current of the best device are 4.59 cm^2/V s, 20.82 V, 1.30 V/decade, 2.10×10^7, 1.40×10^{-11} A, respectively.

Fig. 5 shows the variations of electrical parameters related to the active layer thickness. The subthreshold voltage swing, S, which is in effect a measure of the rate at which a device "turns on" [20], decreases with d, as shown in Fig. 5a. The S value is an indicant of the total states (N_t) including deep bulk states of the a-IZO semiconductor itself and interface states at or near the inter-

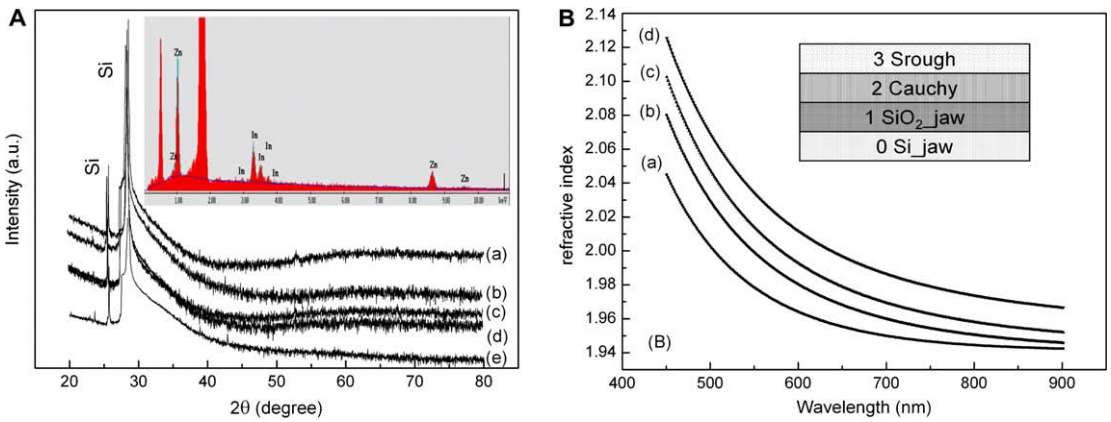

Fig. 2. XRD patterns and spectra of refractive index of IZO thin films with different thickness of post-RTA-treated (a) 33 nm, (b) 61 nm, (c) 88 nm, (d) 114 nm and as-deposited (e) 114 nm. The insets shows EDX pattern of post-RTA-treated 114 nm thick film in (A) and dispersion model for SE date analysis in (B).

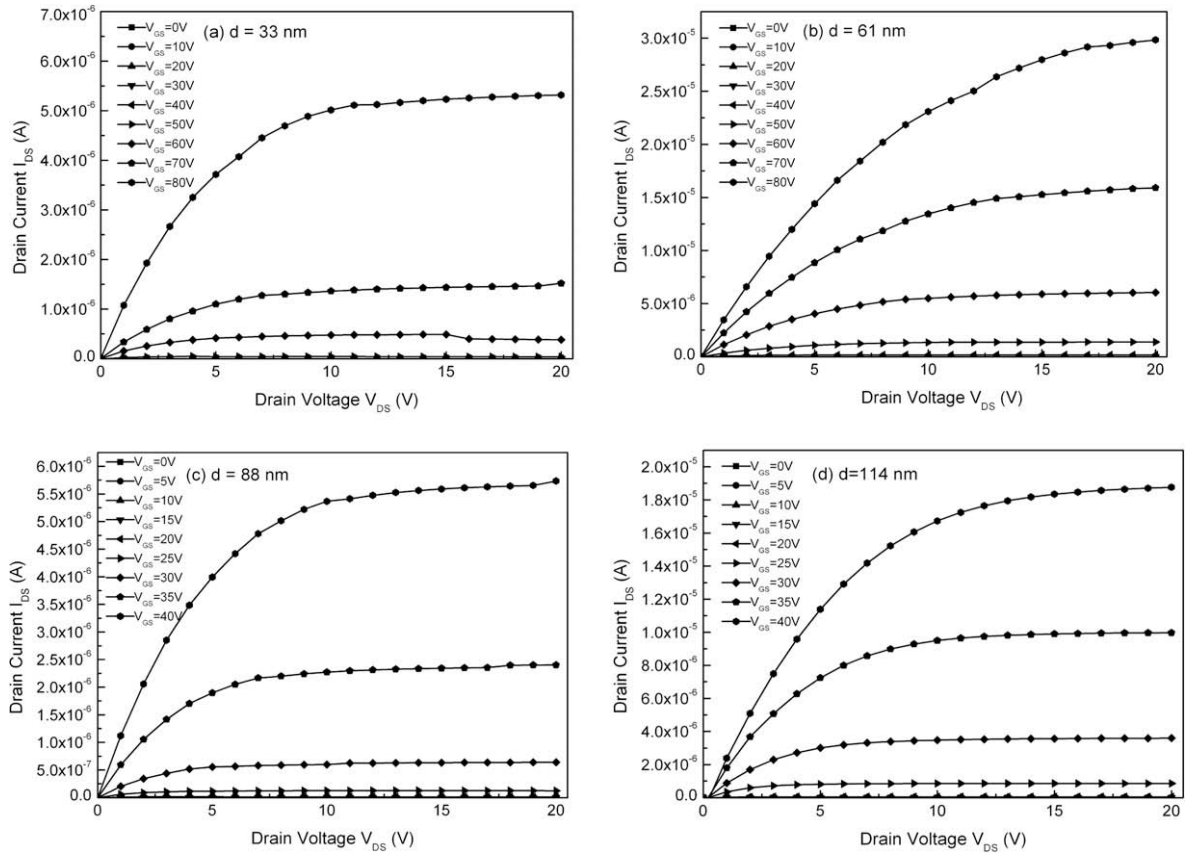

Fig. 3. Output characteristics of the TFTs with channel thicknesses of (a) 33 nm, (b) 61 nm, (c) 88 nm and (d) 114 nm.

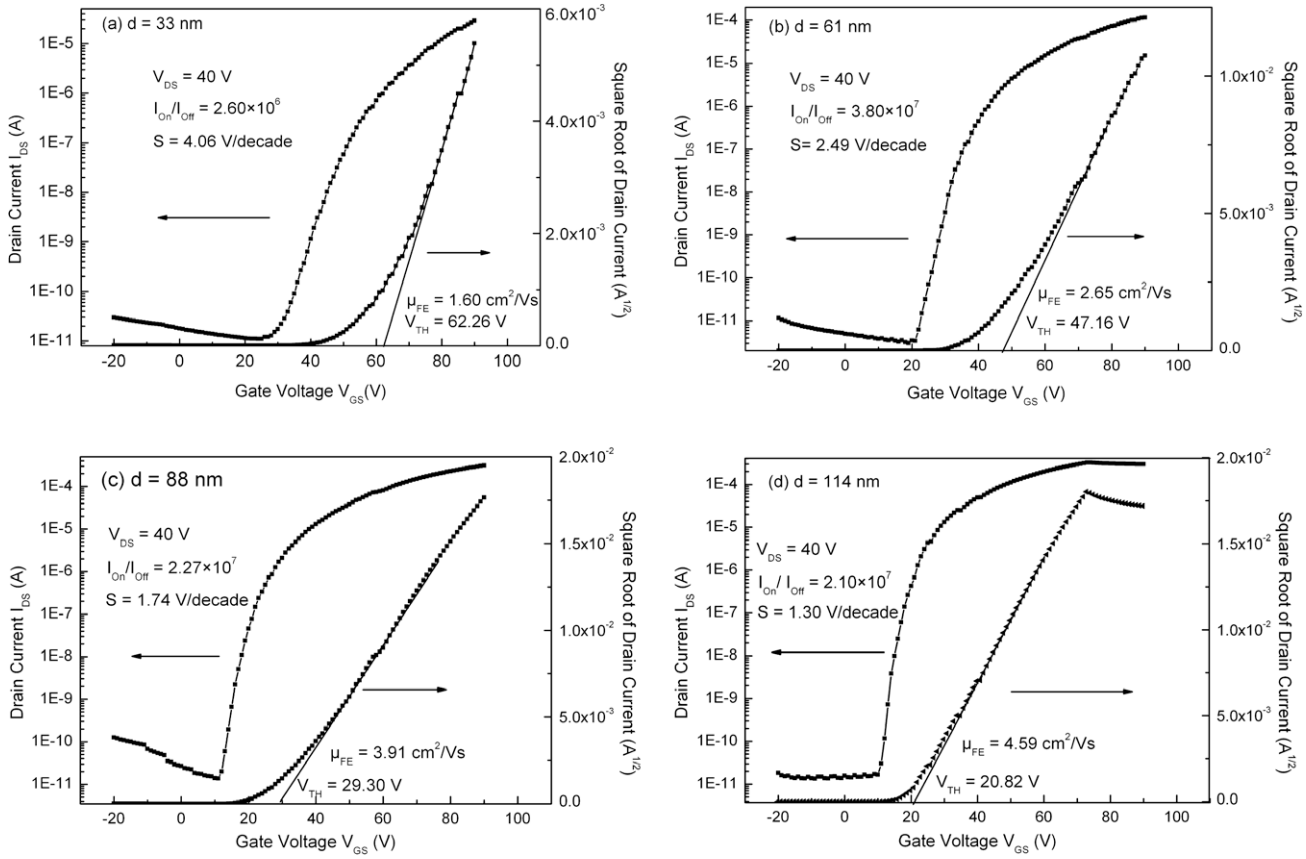

Fig. 4. Transfer characteristics and $I_{DS}^{1/2} - V_{GS}$ of the TFTs at a fixed V_{DS} = 40 V with channel thicknesses of (a) 33 nm, (b) 61 nm, (c) 88 nm and (d) 114 nm.

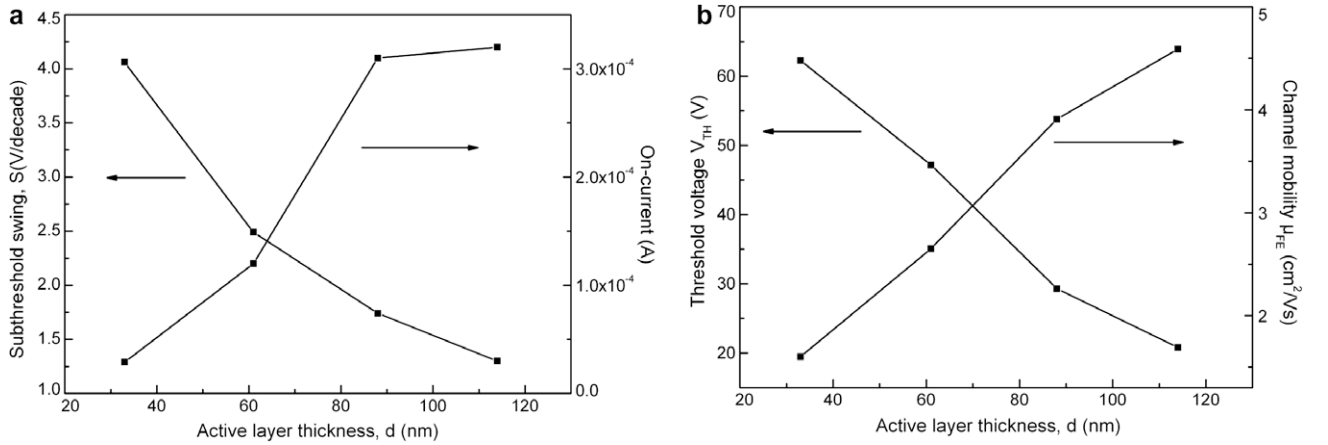

Fig. 5. Variation of electrical parameters related to the active layer thickness: (a) threshold voltage and on-current; (b) channel mobility and subthreshold swing.

face between a-IZO and SiO_2. The subthreshold voltage swing is linked to N_{bs} and N_{ss} by [21].

$$S = \frac{kT}{q\log(e)}\left[1 + \frac{q}{C_i}\left(\sqrt{\varepsilon_s N_{bs}} + qN_{ss}\right)\right] \quad (3)$$

where N_{bs} and N_{ss} are the bulk trap density (cm^{-3}) and the interface trap density (cm^{-2}), respectively, ε_s the semiconductor dielectric constant, q the absolute value of the electron charge, k the Boltzmann constant, and T the temperature. From Eq. (3), it is speculated that the TFTs with thicker channel layers have a lower number of N_t. However, it is necessary to clarify whether N_{bs} or N_{ss} is the main contributor to reduction in the subthreshold voltage swing for the devices with the increase of film thickness. Since the deposition condition for a-IZO films are the same except the deposition time, all devices having the same or similar interface should have similar S. Therefore, the superior S parameter for devices with thicker films suggests that the improvement in the S value stems from the reduction of N_{bs} rather than that of N_{ss}. It is concluded that N_{bs} decreases with increasing d, which is attributed to the densification of the thicker a-IZO films in our case [22].

As shown in the Fig. 5b, the V_{TH} of the devices decreases with d. This could be ascribed to the free carrier density in the channel layer. As there are deep bulk states and interface states, lots of carriers are captured in these states, which cannot contribute to form conductive channels in TFTs. The free carrier density could be obtained from the following equation:

$$n = n_0 - (N_{bs} + N_{ss}/d) \quad (4)$$

where n is the free carrier density (cm^{-3}), n_0 ($>n$) the initial carrier density (cm^{-3}). It has been reported that the carriers are produced from oxygen vacancies according to the equation $O_x^0 \rightarrow \frac{1}{2}O_2(g) + V_O'' = 2e'$ [23,24]. Since the deposition conditions for a-IZO films are the same except the deposition time, n_0 and N_{ss} should be independent of d. As the films thickness increases, the value of $(N_{bs} + N_{ss}/d)$ decreases, as discussed in the upper paragraph. Thereby, the free carrier density (n) increases with d. Consequently, the formation of a conductive channel at the interface is acquired with lower gate voltages in thicker films. Barquinha et al. [16] also believed that this phenomenon was related to a higher number of free carriers in the bulk of the thicker films, thus resulting in an easier accumulation of charges at the interface between semiconductor and dielectric, which is consistent with the observed increase in the on-current for those films (shown in Fig. 5a).

It is believed that the field-effect mobility has relations to the free carrier density [25]: $\mu_{FE} \approx (n/n_0) \times \mu_0$, where μ_0 is the free carrier mobility in the extended states. Since n increases with d, the μ_{FE} is smaller in the TFTs with smaller d, as observed in Fig. 5b. Besides, the μ_{FE} is also related closely to scattering at the semiconductor/dielectric interface. Fig. 6 shows the variation of gate voltage V_{GS} and transverse electric field intensity E with the active layer thickness obtained at V_{DS} = 40 V and $I_{DS} = 1 \times 10^{-5}$ A. As seen in the Fig. 6, the TFTs with the thinner films need higher gate voltage V_{GS} to reach the same saturation condition ($I_{DS} = 1 \times 10^{-5}$ A). As the gate voltage increases, carriers in the accumulation layer withstand a larger transverse electric field, so that they are attracted closer to the a-IZO/SiO_2 interface where they experience more intensely scattering due to the roughness of the interface [26]. In a word, it is concluded that the μ_{FE} would increase in the TFTs with increasing d.

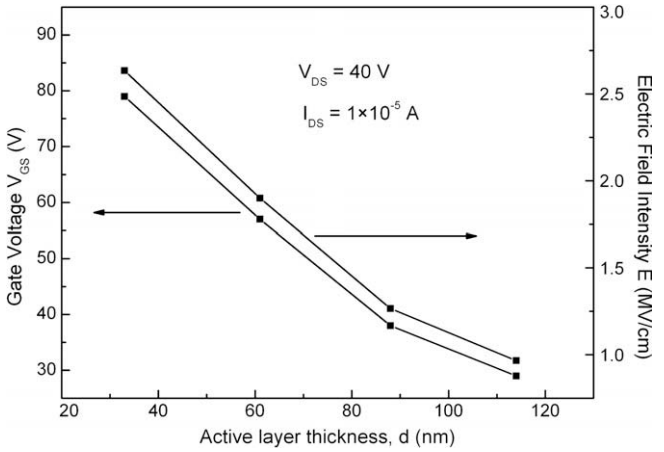

Fig. 6. Variation of gate voltage and transverse electric field intensity related to the active layer thickness obtained at V_{DS} = 40 V and $I_{DS} = 1 \times 10^{-5}$ A.

4. Conclusion

In this work, a-IZO thin-film transistors were fabricated with different thick channel layers. The as-deposited and RTA-treated IZO thin films are found to be amorphous. It is noted that the properties of devices got better with increasing the active layer thickness, in the range of 33–114 nm. We believed that this phenomenon was induced by the free carrier and interface scattering. It is concluded that the semiconductor thickness plays a vital role on the electrical performances of TFTs based on a-IZO. In addition, it was noted the electrical performance of a-IZO TFT exceeded the conventional a-Si TFT, especially the high saturation mobility

($\sim$4.59 $cm^2/V\,s$). Therefore, a-IZO is a very good candidate for the active layer of TFTs.

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