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Self-assembled dual in-plane gate thin-film transistors gated by nanogranular SiO_2 proton conductors for logic applications

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Phosphorus (P)-doped nanogranular SiO_2 films are deposited by plasma-enhanced chemical vapor deposition at room temperature, and a high proton conductivity of $\sim 5.6 \times 10^{-4}$ S cm^{-1} is measured at room temperature with a relative humidity of 70%. The accumulation of protons at the SiO_2/indium-zinc-oxide (IZO) interface induces a large electric-double-layer (EDL) capacitance. Thin-film transistors (TFTs) with two in-plane gates are self-assembled on transparent conducting glass substrates. The large EDL capacitance can effectively modulate the IZO channel with a current ON/OFF ratio of $>10^7$. Such TFTs calculate dual input signals at the gate level coupled with a floating gate, analogous to that of neuron MOS (*v*MOS). AND logic is demonstrated on the neuron TFTs. Such neuron TFTs gated by P-doped nanogranular SiO_2 shows an effective electrostatic modulation on conductivities of oxide semiconductors, which is meaningful for portable chemical-biological sensing applications.

Introduction

Multi-gate devices have been proposed as a viable solution to complementary metal-oxide-semiconductor (CMOS) scaling issues.[1] More functions could be introduced to a single device through a multi-independent gate, thereby increasing the functional density for a given area. Multi-gate thin-film transistors (TFTs) have also attracted a lot of attention in chemical and biological sensing, pixel display drivers and logic circuit applications.[2–7] In 1992, a highly functional neuron MOS (*v*MOS) transistor was proposed, which possesses a continuous floating gate and multiple input control gates, capacitively coupled together with the floating gate.[8] Such a device calculates the weighted sum of all input signals at the gate level, and controls the "on" and "off" states of the transistor. The so-called *v*MOS transistor has been designed for different applications, such as D/A and A/D converters,[9] sensors,[10,11] analog multipliers,[12] and so on. The unique feature of the neuron transistor is that almost no power dissipation occurs during the calculation due to the gate-level sum operation in a voltage mode using the capacitive coupling effect. However, due to the multiple gate/dielectric deposition and precise photolithography steps, the fabrication of such *v*MOS transistors by the standard CMOS process is expensive and time-consuming.

On the other hand, as another family of transistors, electrochemical transistors have been proposed to be gated by polymer-based electrolytes,[13–17] meaningful for some applications, including displays, sensors, actuators and low cost memory, *etc.* Field-effect gating using ionic liquid electrolytes or gel electrolytes could effectively cause the electrostatic field to dope the conducting polymer and inorganic semiconductor, leading to a higher carrier density.[18] Therefore, the transistors could typically operate using a low drive voltage of <2 V. The movements of the anions/cations in the electrolyte towards the positively/negatively charged electrode form an electric-double-layer (EDL), composed of a compact Helmholtz layer and a diffuse layer.[19–21] As a result of the charge separation within a few angstroms, such EDL capacitors could have a high capacitance up to ~ 500 μF cm^{-2},[22] as is highly desirable for low-energy consumption applications. Recently, various EDL FETs have been developed, including organic,[23,24] carbon nanotubes,[25] and inorganic semiconductors,[26] and have also been studied from the view point of sensor applications using aqueous electrolytes, *e.g.*, ion-sensitive FETs.[27,28] Recently, electrostatic modulation of the conductivities of wide band-gap oxide semiconductors has been realized by inorganic electrolytes.[29–32] However, high proton conductivity in such inorganic electrolytes has not been addressed yet. Moreover, multi-gate applications for the inorganic electrolyte gated TFTs are highly desirable for potential applications in chemical-biological sensing, logic applications and so on.

Here, our experimental results demonstrate that phosphorus-doped nanogranular SiO_2 films shows a high proton conductivity and a large electric-double-layer (EDL) capacitance. In-plane gate devices were self-assembled on transparent conducting glass substrates. A high EDL capacitance can effectively modulate the indium-zinc-oxide (IZO) channel. Dual in-plane gate coupled with the bottom FTO floating gate controlling the

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"on" and "off" of the TFT are analogous to that of neuron MOS (νMOS).[8] Such inorganic neuron TFTs exhibit a large field-effect mobility (10 cm^2 V^{-1} s^{-1}), a high current ON/OFF ratio (>10^7) and a small sub-threshold swing (100 mV per decade). AND logic is realized on such neuron TFTs.

Experimental detail

P-doped nanogranular SiO_2 films were deposited by plasma-enhanced chemical vapor deposition (PECVD) using SiH_4 (95% SiH_4 + 5% PH_3) and O_2 as reactive gases. Nanogranular SiO_2 films deposited on polished Si wafers received a cross-sectional morphology characterization by field-emission scanning electron microscopy (FE-SEM) (Hitachi-S4800). Nanogranular SiO_2 films deposited on Cu grids received TEM measurements by a FEI-TECNAI F20-TEM system. The proton conductivities and frequency dependent capacitances of such films were characterized by a Solartron 1260A Impedance/Gain-Phase Analyzer. TFTs were fabricated with a self-assembled process through a shadow mask. The indium-zinc-oxide (IZO) films for source/drain electrodes were deposited on the nanogranular SiO_2 film coated FTO glass substrate by RF sputtering IZO target in Ar ambient, where the FTO layer on the glass substrate works as a floating gate. The radio frequency (RF) power, Ar flow rate and the chamber pressure were set to be 100 W, 14 sccm and 0.5 Pa, respectively. A thin IZO channel could be self-assembled between the IZO source/drain electrodes due to the diffraction effect, as shown in Fig. 1a. The channel length (L) is 80 μm and the channel width (W) is 1 mm. Fig. 1b shows the optical transmission spectrum of the entire TFT arrays on the glass substrate in the wavelength range between 200 and 1000 nm. The average transmittance in the visible range (400–800 nm) is about 70%, indicating that the TFTs are transparent to visible light. The IZO source/drain and dual in-plane gates (G1 and G2) were simultaneously deposited by RF-magnetron sputtering through the same shadow mask. For the entire device fabrication processes, no lithography step was used. The electrical transport and logic operation of the in-plane gate TFTs were recorded by a semiconductor parameters characterization system (Keithley 4200 SCS).

Results and discussion

Fig. 2a shows the cross-sectional scanning electron microscopy (SEM) images of the P-doped nanogranular SiO_2 films on a Si substrate. Clear nanocolumnar microstructures with aligned nanochannels are observed in the nanogranular SiO_2 films deposited at room temperature. The thickness of the nanogranular SiO_2 films is estimated to be ~720 nm. Fig. 2b shows the TEM images of the nanogranular SiO_2 films deposited on a Cu grid. The dark region shows the SiO_2 grains, while the bright region shows the isolation between the grains, showing that the width of the aligned nanochannels observed in the SEM

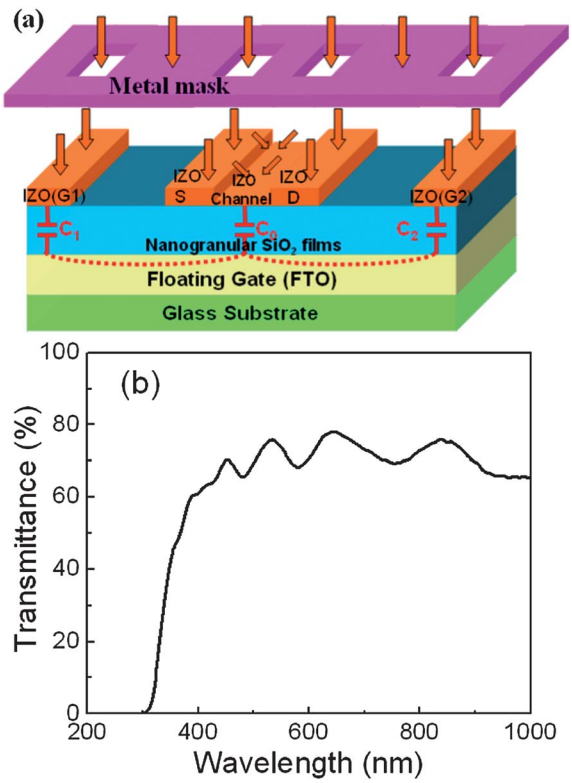

Fig. 1 (a) A schematic diagram of the dual in-plane gate TFTs with a self-assembled IZO active channel through mask diffraction. (b) The optical transmittance spectrum of the IZO TFTs arrays on a FTO glass substrate.

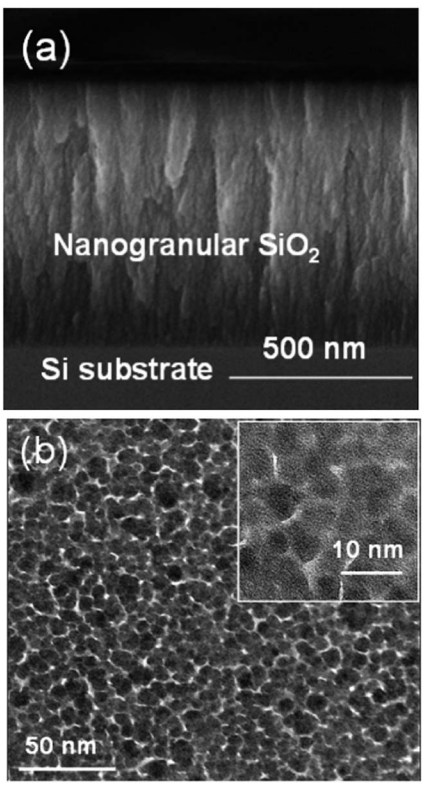

Fig. 2 (a) A cross-sectional SEM image of the as-deposited P-doped nanogranular SiO_2 films. (b) TEM image of the as-deposited P-doped nanogranular SiO_2 films on Cu grids. The inset shows the magnified view with a high resolution image.

measurements is ~2 to 5 nm. Such aligned nanochannels allow proton movement within the channels . The magnified view of the nanogranular SiO_2 films shows that the size of the SiO_2 grain is ~10 nm. Therefore plenty of the nanochannels are formed in the as-deposited nanogranular SiO_2 layer, which is favorable for high proton conductivity and high EDL capacitance.

The proton conductivities of the P-doped nanogranular SiO_2 films are determined from Cole–Cole plots by an AC method using a Solartron 1260A impedance analyzer at the relative humidity (RH) of 70%. Impedance spectroscopy data are collected as real (Re Z′) and imaginary (Im Z″) components of the complex impedance, as shown in Fig. 3a. The impedance real value (R) of 114.8 Ω is obtained with the impedance imaginary value equal to zero. The conductivity (σ) could be obtained from the relation below:[33]

$$\sigma = \frac{D}{(R - R_0)A}$$

where D, A and R_0 are the thickness of the proton conductor, electrode surface area, and the resistance of the electrodes, respectively. The thickness D is ~720 nm, A is ~1.5 × 10^{-3} cm^2, while R_0 is measured to be ~30 Ω. Therefore, the conductivity (σ) is estimated to be ~5.6 × 10^{-4} S cm^{-1}, which is much higher than the conductivity of 10^{-8} S cm^{-1} for porous SiO_2 without exposure to the atmosphere, strongly indicating protonic transport to be dominant.[34,35] Such SiO_2 proton conductors have been used in non-volatile memory devices[36] and ion-current diodes.[37]

On the one hand, hydrogen dissociated from SiH_4 and PH_3 during the PECVD process can enter the nanogranular SiO_2 matrix as Si–OH^+ and P–OH^+. On the other hand, the nanogranular SiO_2 films exposed to the atmosphere absorb H_2O molecules in the nanoholes and the nanochannels,[35] which hydrogen bond with the hydroxyl groups.[38] Fig. 4 schematically illustrates the proton hopping process. When biasing the nanogranular SiO_2 films on the IZO electrodes, the unstable bond between hydrogen and oxygen will easily break up, resulting in mobile protons of H^+. The proton conductivities are associated with a sequence of proton hopping between hydroxyl groups and water molecules.[33,38,39] High conductivities indicate that the absorbed water facilitates the proton conductivities. With the external electric field in the nanogranular SiO_2 films, an oriented transport of protons along the electric field through a sequence of hops results in the accumulation of protons at the SiO_2/IZO interface (bottom FTO positively biased), where they result in large image charges with equal densities and an opposite sign in the other side of the interface. Thus, a so-called electric-double-layer (EDL) is formed as the equilibrium state. The specific capacitance–frequency curves for the nanogranular SiO_2-based proton conductor are also illustrated in Fig. 3b from 1 Hz to 10 MHz. The capacitance increases with decreasing frequency. A maximum specific capacitance of 2.5 μF cm^{-2} is obtained at 1.0 Hz due to the formation of the electric-double-layer (EDL) at the proton conductor/IZO interface. The leakage current is less than 5 nA (inset in Fig. 3b). The results here strongly indicate that the room temperature deposited P-doped nanogranular SiO_2 films are an electronically insulating but proton-conducting solid electrolyte. The EDL formed at the interface induces a rather large electric field on the order of megavolts per centimeter at the EDL region, resulting in a high density of charge carriers at the surface of the IZO channel. Such an electrostatic modulation process controls the

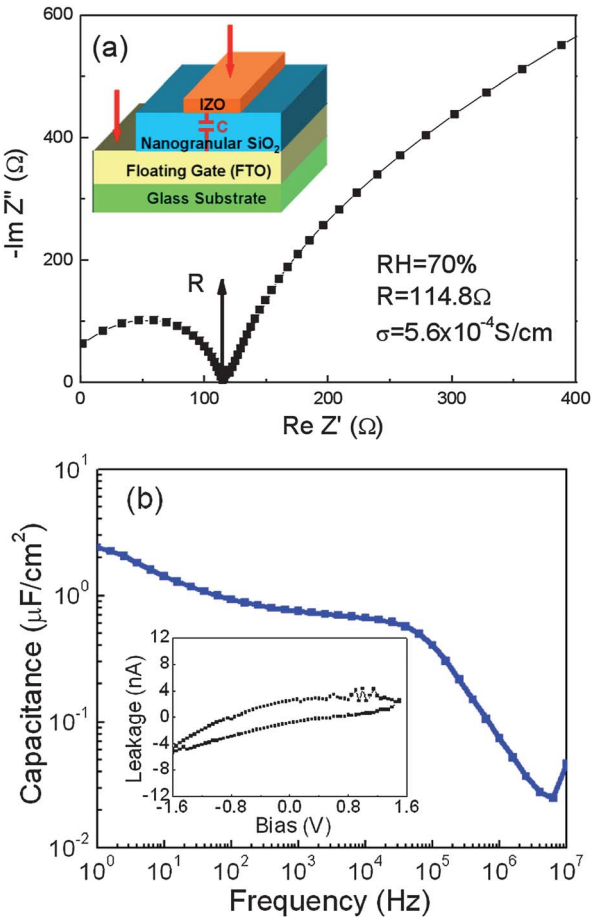

Fig. 3 (a) The proton conducting characteristics of the P-doped nanogranular SiO_2 films: Cole–Cole plots. Inset: The sample structure. (b) The specific capacitance–frequency curves for the nanogranular SiO_2 films using an IZO/SiO_2/bottom FTO structure. Inset: The leakage of the nanogranular SiO_2 films.

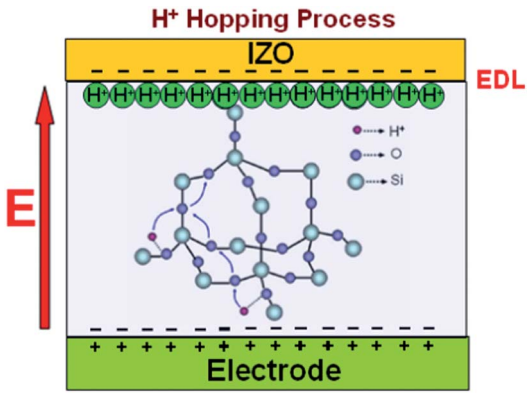

Fig. 4 The proton H^+ hopping mechanism in nanogranular SiO_2 films.

conductance of the IZO channel layer, which is meaningful for low-voltage electrostatic modulation devices.

For the in-plane gate IZO TFTs fabricated here, there is one bottom continuous floating gate and two top in-plane gates. When taking the bottom floating FTO layer as a normal bottom gate, then a normal bottom gate IZO TFT is obtained, as shown in the inset of Fig. 5. Fig. 5 shows the transfer characteristics of the bottom gate IZO TFT gated by P-doped nanogranular SiO_2 films with a constant drain-source bias of 1.5 V. The sub-threshold swings (S), current ON/OFF ratio and threshold voltage are estimated to be 100 mV per decade, 2×10^7 and -0.6 V, respectively. Therefore, the device works in a depletion mode. The field-effect electron mobility (μ) at the saturation region is estimated to be $\sim$10 cm^2 V^{-1} s^{-1} by the following equation:

$$I_{ds} = \frac{WC_0}{2L}\mu(V_{gs} - V_{th})^2$$

On the fabricated dual in-plane gate IZO-based TFTs, as shown in Fig. 1a, the dual in-plane gates (G1 and G2) are capacitively coupled through the bottom floating gate (FTO) with capacitances of C_1 and C_2, analogous to that of neuron MOS (νMOS).[8] The coupling effects of the two in-plane gates are overlapped in the bottom floating gate where the effective charge accumulation is a superposition of dual in-plane gate biases modified by their capacitances. Therefore, the TFT fabricated here is a neuron TFT. Since the capacitances (C_1 and C_2) are equal to the EDL capacitance (C_0) of the nanogranular SiO_2 proton conductors, G1 and G2 work as inputs with the same weight. Fig. 6 illustrates the transfer characteristics of the dual in-plane gate IZO neuron TFTs at the saturation region. The drain-source bias is kept at 1.5 V. The inset in Fig. 6 shows the optical microscope image of the fabricated device. The distance between the in-plane gate and the source/drain is 300 μm and the channel width/length is 1000 μm/80 μm. The drain current is controlled by two gates (G1 and G2). G1 bias sweeps from -2 V to 1 V with the fixed G2 bias set to 0 V or 2 V. A bias of -2 V is denoted as the LOW state, *i.e.*, "0" state, and a bias of 0 V as the HIGH state, *i.e.*, "1" state. When one in-plane gate biases "0" (*i.e.*, "00", "01", or "10"), only a low drain current of <100 pA is measured, *i.e.*, the device is in an OFF state. When both the dual in-plane gate bias "1", a high drain current of >50 μA is measured, *i.e.*, the device is in an ON state.

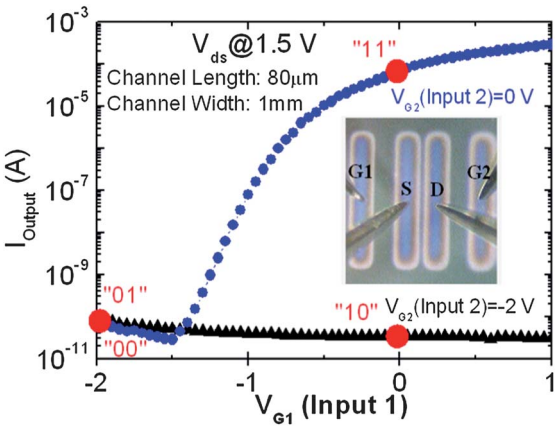

Fig. 6 Transfer curves (I_{ds}–V_{gs}) for the dual in-plane gate IZO neuron TFTs with the second in-plane-gate biased at 0 V or -2 V.

For the dual in-plane gate IZO neuron TFTs, the current is controlled by a depletion region created by the two gates, as shown schematically in Fig. 7. In the OFF state, the depletion regions fill the channel completely, leading to a low OFF current. In the ON state, the depletion region disappears, and a conducting path is created for the current to flow in the channel. With a high specific capacitance of the P-doped nanogranular SiO_2 proton conductor, one in-plane gate is enough to keep the entire oxide channel depleted when it is biased LOW, even when the other gate is biased HIGH. Therefore, both gates are required to be HIGH in order to change the dual in-plane gate neuron TFTs to an ON state, resulting in an AND Logic.

The equivalent logic circuit of the dual in-plane gate neuron TFT is shown in Fig. 8a. The devices are characterized by applying different fixed bias directly and independently to each of the two gates (input 1 and input 2), corresponding to two

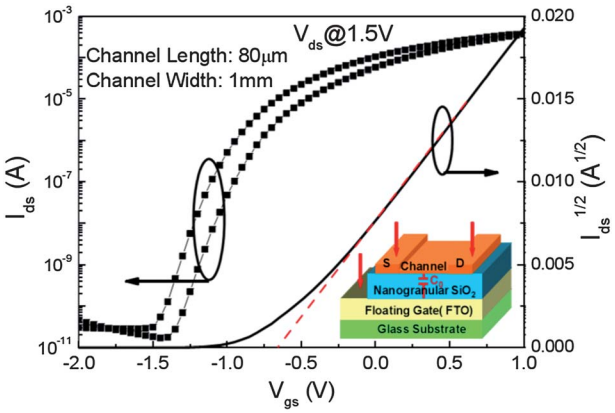

Fig. 5 Transfer characteristics of the bottom gate IZO TFT gated by nanogranular SiO_2 films. Inset: the IZO TFT structure.

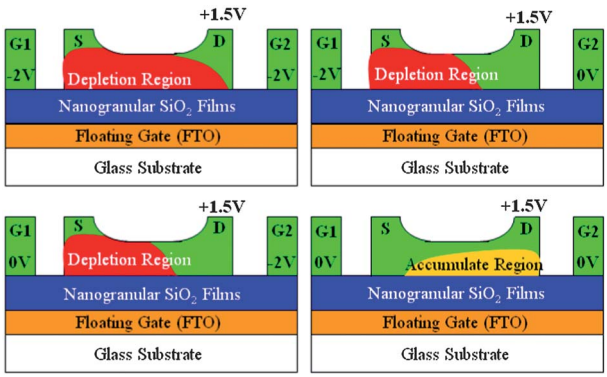

Fig. 7 Schematic images of the dual in-plane gate IZO neuron TFT showing the depletion regions (in red) formed under different biases, illustrating AND logic.

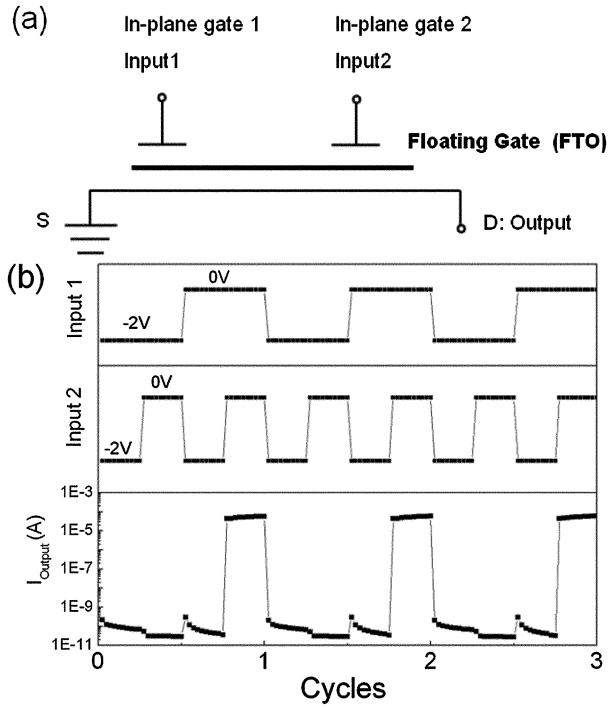

Fig. 8 (a) The logic circuit diagram of the dual in-plane gate neuron TFT. (b) Input–output characteristics of the AND logic from the dual in-plane gate IZO neuron TFTs.

logic states. The in-plane gate logic operates as an AND-gate, demonstrated in Fig. 8b. A HIGH input level (0 V) is defined as the gate voltage that is needed to open the channel (logic 1), and a LOW input level (−2 V) is defined as the gate voltage that is needed to switch off the channel (logic 0). The channel current that flows between source and drain is detected as the output. When both inputs are "1", the device conductance is high ON. When either or both inputs are "0", the device conductance is low OFF. The modulation, *i.e.*, the ON/OFF ratio of $>10^5$ between the two logic states is achieved, indicating that the operation of this logic gate is robust. The AND logic is useful in applications, such as sensor arrays,[40,41] or to control the luminescence of organic light-emitting transistors,[42] *etc.*

Conclusion

In summary, a high room temperature proton conductivity of 5.6×10^{-4} S cm^{-1} and a large electric-double-layer capacitance of 2.5 μF cm^{-2} were observed in P-doped nanogranular SiO_2 films deposited by a PECVD method at room temperature. Transparent IZO-based dual in-plane gate TFTs were self-assembled on an inorganic proton conductor at room temperature. The IZO channel could be effectively modulated by the dual in-plane gates through a floating gate, analogous to that of neuron MOS (*v*MOS). AND logic operation was demonstrated on such neuron TFTs. Fully oxide-based low-voltage, transparent neuron TFTs may find applications in chemical sensing and bioelectronics.

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