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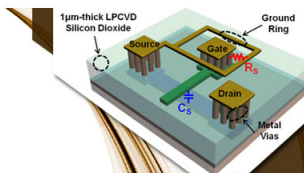
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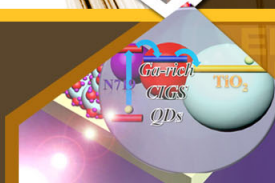
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Laser directly written junctionless in-plane-gate neuron thin film transistors with AND logic function

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Junctionless oxide-based neuron thin-film transistors with in-plane-gate structure are fabricated at room temperature by a laser scribing process. The neuron transistors are composed of a bottom indium-tin-oxide floating gate and multiples of in-plane control gates. The control gates, coupling with the floating gate, control the “on” and “off” of the transistor. Effective field-effect modulation of the drain current has been realized. AND logic is demonstrated on a dual in-plane gate neuron transistor. The developed laser scribing technology is highly desirable in terms of the fabrication of high performance neuron transistors with low-cost. © 2013 American Institute of Physics.

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Multigate devices have been proposed as a viable solution to complementary metal-oxide-semiconductor (CMOS) scaling issues.¹ More functions could be introduced in a single device through multi-independent gate, therefore increasing the functional density for a given area. Dual-gate thin-film transistors (TFTs) have attracted a lot of attentions in chemical and biological sensing, pixel display driver, and logic circuit applications.^{2–6} A highly functional MOS transistor called neuron MOS transistor has been developed by executing a weighted sum calculation of multiple input signals and then controls the “on” and “off” states of the transistor, thus realizing the neuron function.^{7–9} The device has a floating gate and multiple input control gates which are capacitively coupling with the floating gate, featuring a full compatibility with standard CMOS process. However, due to the multiple gate/dielectric deposition and precise photolithography steps, the fabricating of such neuron transistors by standard CMOS process is expensive and time-consuming. Recently, the concept of junctionless transistors has been proposed and explored.^{10–12} Compared with the conventional field-effect transistors (FETs), the unique features of such junctionless transistors is that the channel doping is the same or comparable to that of the source and drain (S/D), therefore no sour/drain junction formation steps are needed, and the carrier transport is less sensitive to the channel interface. However, fabrication of these junctionless FETs is still rather challenging. As an interesting concept for promising functional devices, in-plane gate transistors have been developed as logic devices,¹³ rectifier,^{14,15} negative differential resistance devices,¹⁶ etc. Laser scribing process was also proposed for source/drain patterning.^{17,18} However, masks are still needed during the TFTs fabrication.

In this work, a laser scribing method without any masks and photolithography is developed to directly write the junctionless in-plane-gate neuron TFTs arrays on glass substrates at room temperature. SiO₂-based solid electrolyte works as gate dielectrics.^{19,20} The channel and source/drain electrodes

are realized by a thin indium-tin-oxide (ITO) layer without any intentional source/drain junction. The bottom ITO layer works as a floating gate, while the top isolated ITO works as the in-plane control gate. Effective field-effect modulation of the drain current has been realized on both the single in-plane-gate (SG) mode and the dual in-plane-gate (DG) mode. Good electrical performance has been exhibited on SG neuron TFT: low OFF current of <3 pA, high I_{on}/I_{off} ratio of >10⁶, high electron mobility of ~12.6 cm²/Vs, and low subthreshold swing of 0.25 V/dec. AND logic was experimentally demonstrated on the DG neuron TFT. The developed laser scribing technology is highly desirable in terms of the low-cost fabrication process.

Fabrication of ITO junctionless in-plane gate neuron transistors was performed at room temperature, as schematically shown in Figs. 1(a) and 1(b). After cleaning the substrates, a 100-nm-thick Al thin film was deposited on ITO surface by sputtering. Then, a 2-μm-thick SiO₂-based solid electrolyte film was deposited by plasma enhanced chemical vapor deposition (PECVD) using SiH₄ and O₂ as reactive gases. Finally, a 25-nm-thick ITO films were deposited on the SiO₂-electrolyte based gate dielectrics by sputtering. The ratio frequency (RF) power, Ar flow rate, and the chamber pressure were set to be 100 W, 14 sccm, and 0.5 Pa, respectively. Then, the neuron TFTs were fabricated on the prepared stacks of ITO/SiO₂-electrolyte/Al/ITO/glass substrates by adopting a laser scribing process. The focused laser beam selectively etches out the deposited thin films due to a localized thermoelastic force caused by rapid thermal expansion resulting from the pulsed laser irradiation. The laser patterned ITO arrays are with the dimension of 1 mm × 0.2 mm. The capacitors (C1, C2, C3, ..., Cn) are effectively coupled through bottom ITO floating gate, as shown in Fig. 1(c). The source and drain are obtained on the same ITO region, while the isolated ITO region works as the in-plane control gate. When set signals on G1 (or G1 and G2), the junctionless SG (or DG) neuron TFT is obtained. The capacitance-frequency measurement of the SiO₂-based solid electrolyte was performed using an impedance analyzer. The electrical characteristics of the junctionless SG and DG TFTs were measured

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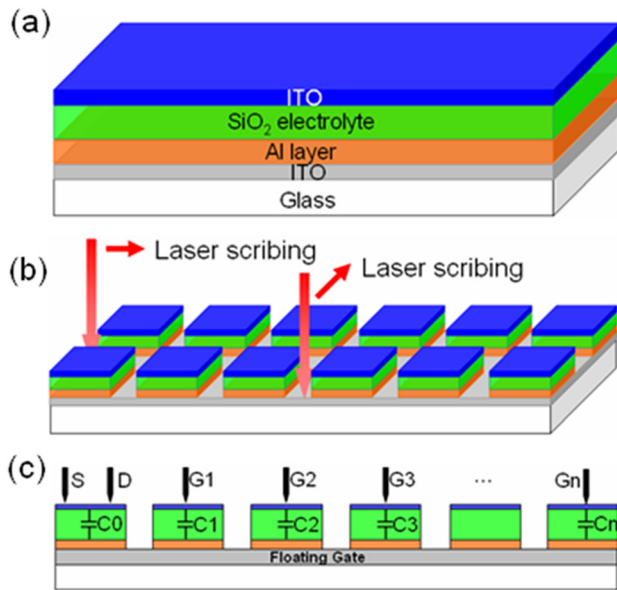


FIG. 1. (a) The obtained ITO/SiO₂-electrolyte/Al/ITO/Glass stack. (b) Laser scribing process results in the isolation of the top ITO films as well as the SiO₂-electrolyte and Al layer. (c) Schematic cross-sectional view of the laser patterned junctionless in-plane gate neuron TFTs structure. The capacitors (C1, C2, C3, ..., Cn) are effectively coupled through bottom ITO floating gate.

with a Keithley 4200 SCS semiconductor parameter analyzer at room temperature in the dark.

The output characteristics of the laser patterned junctionless SG neuron TFTs are shown in Fig. 2. The nominal channel length is 0.4 mm, while the channel width is 0.2 mm (as shown in the inset of Fig. 2). At low V_{ds} , the drain current increases linearly with drain voltage, indicating that the device has a good ohmic contact. At the higher V_{ds} , the drain current gradually approaches a saturated value. With a gate voltage of 2 V, the saturation current is observed to be $\sim 5 \mu\text{A}$ at a drain voltage of 2 V.

Fig. 3 shows the transfer characteristics of the junctionless SG neuron TFTs at saturation mode, fixed at V_{ds} of 2 V. It can be found that I_{ds} can be effectively modulated by V_{gs} .

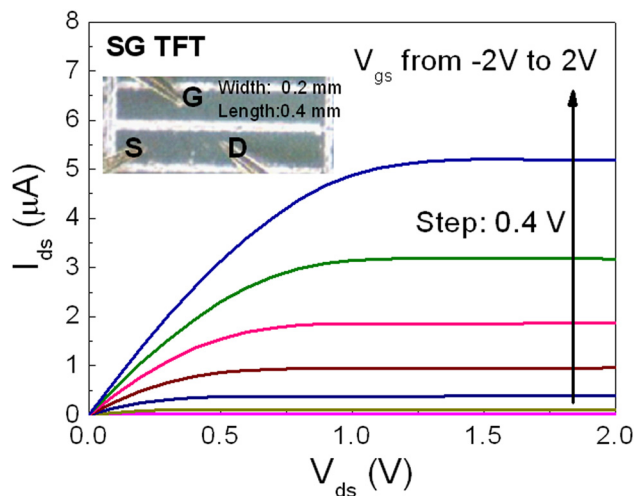


FIG. 2. Output characteristics (I_{ds} vs V_{ds}) of the laser patterned junctionless SG TFTs. Inset: Top view optical image of the junctionless SG neuron TFTs in electrical measurement on a probe station.

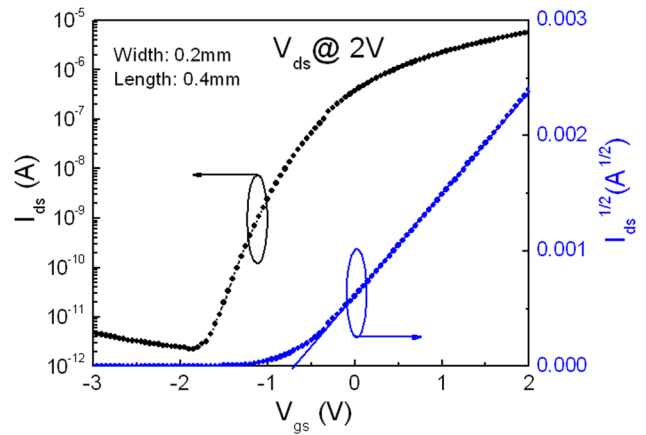


FIG. 3. Transfer characteristics (I_{ds} vs V_{gs} and the square root of I_{ds} vs V_{gs}) of the junctionless SG neuron TFTs at saturation mode, fixed at V_{ds} of 2 V.

The subthreshold swing (S) is found to be $\sim 0.25 \text{ V/dec}$. The drain current on/off ratio I_{on}/I_{off} is determined to be $\sim 3 \times 10^6$. A threshold voltage V_{th} of -0.7 V is estimated by extrapolating the linear portion of the curves relating $I_{ds}^{1/2}$ and V_{gs} to $I_{ds}^{1/2} = 0$. The field-effect mobility (μ) in the saturation region can be extracted from the following equation:

$$I_{ds} = \left(\frac{WC_i\mu}{2L} \right) (V_{gs} - V_{th})^2 \quad (V_{ds} > V_{gs} - V_{th}), \quad (1)$$

where L is the channel length, W is the channel width, and C_i is the unit area capacitance of the dielectrics. Capacitor of SiO₂-based solid electrolyte with two in-plane ITO electrodes was measured using an ITO/SiO₂-electrolyte/Al/ITO in-plane test structure as shown in Fig. 1(c) with G1 and S as the electrode (results not shown here). The in-plane gate capacitance of $0.25 \mu\text{F}/\text{cm}^2$ is used to calculate the field-effect mobility. The field-effect electron mobility is estimated to be $\sim 12.6 \text{ cm}^2/\text{Vs}$.

Fig. 4 shows the transfer characteristics of the junctionless DG neuron TFTs at saturation region, fixed at V_{ds} of 1.5 V. Both the channel width and the channel length is $\sim 0.2 \text{ mm}$ (as shown in the inset of Fig. 4). The drain currents are controlled by two gates (G1 and G2). G1 bias sweeps

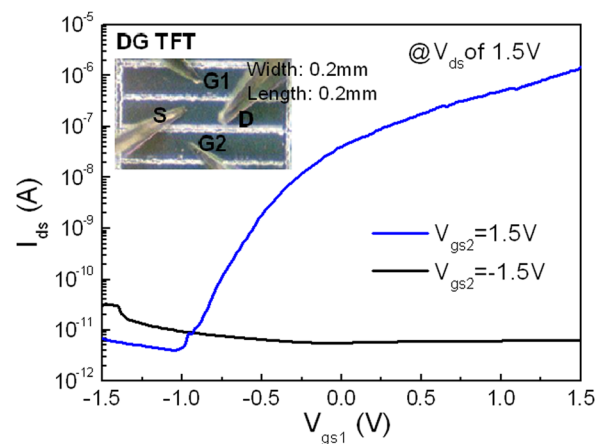


FIG. 4. The transfer characteristics of the junctionless DG neuron TFTs at saturation region, fixed at V_{ds} of 1.5 V. Inset: Top view optical image of the junctionless DG neuron TFTs in electrical measurement on a probe station.

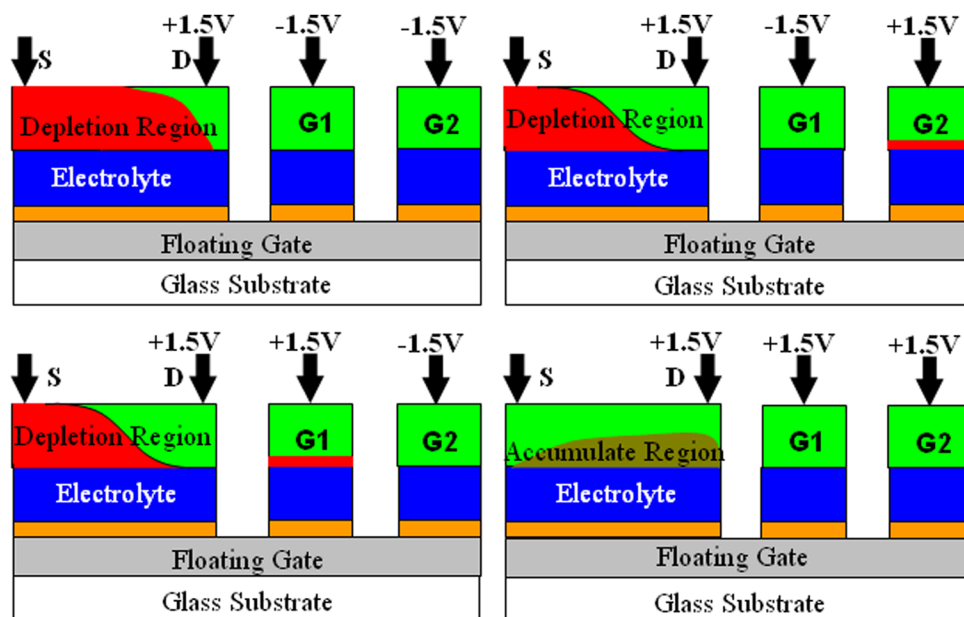


FIG. 5. Schematic images of the dual in-plane control gate ITO neuron TFT showing the depletion regions (in red) formed under different biases, illustrating AND logic.

from -1.5 V to 1.5 V with the fixed G2 bias set to 1.5 V and -1.5 V, respectively. It could be found obviously from Fig. 4 that the drain current could be effectively modulated by G1 bias with fixed G2 bias of 1.5 V. The drain current can be turned on or off effectively with the drain current on/off ratio $I_{\text{on}}/I_{\text{off}}$ of above 10^5 . The subthreshold swing (S) and the threshold voltage (V_{th}) are found to be ~ 0.25 V/dec and -0.25 V, respectively. On the other hand, the drain current cannot be turned on effectively under G2 bias of -1.5 V. The drain current is controlled by depletion region created by the two control gates as shown in Fig. 5. For example, when G2 is negative biased at -1.5 V, electrons in the ITO channel will be depleted, resulting in a low OFF drain current. At the same time, since G1 is also ITO film with same thickness as the channel, it would also be depleted. Then, the value of gate capacitance would be decreased due to the depletion capacitor in series, and the electrostatic coupling ability of G1 decreases. So such TFTs cannot be turned on by G1 when G2 is biased -1.5 V. While when both the control gates are biased $+1.5$ V, the ITO channel works in accumulate region, resulting in a high ON current. Such DG neuron TFT performances are meaningful for logic gate applications.

The logic circuit of a DG neuron TFT is shown in Fig. 6(a). The devices are characterized by applying different fixed potentials, corresponding to two logic states, HIGH state (“1”) at 1.5 V and LOW state (“0”) at -1.5 V, input directly and independently to each of the two control gates (see the logic circuit diagram for input 1 and input 2). This in-plane gate logic operates as an AND gate as demonstrated in Fig. 6(b). The drain current monitored are also detected as output (“1”: I_{ds} above $0.1 \mu\text{A}$; or “0”: I_{ds} below $0.01 \mu\text{A}$). At “00,” “01,” or “10,” the device is in the OFF state. A low OFF current of <0.01 nA is measured. For state “11,” the device is ON with a HIGH current of $>0.7 \mu\text{A}$. The results indicate a high ON/OFF ratio of $\sim 10^4$ between the two logic states. Though there are some small noises of below 0.1 nA, the HIGH/LOW ratio output is still over 10^3 . The HIGH/LOW ratio is high enough for reliable logic operations.

In summary, a simple laser scribing process without any mask and photolithography is implemented in fabricating junctionless in-plane gate neuron TFT arrays. Such junctionless neuron TFTs feature that the channel and the source/drain electrodes are of the same ITO films without any intentional source/drain junction formation steps. The bottom ITO layer works as a floating gate, while the top isolated ITO works as the in-plane control gate. The control gates, coupling with the floating gate, control the “on” and “off” of the transistor. Effective field-effect modulation of the drain current has been realized on both the SG mode and the DG mode. AND logic is demonstrated on a dual in-plane gate neuron transistor with a high HIGH/LOW ratio, allowing the reliable logic operation. The developed laser scribing

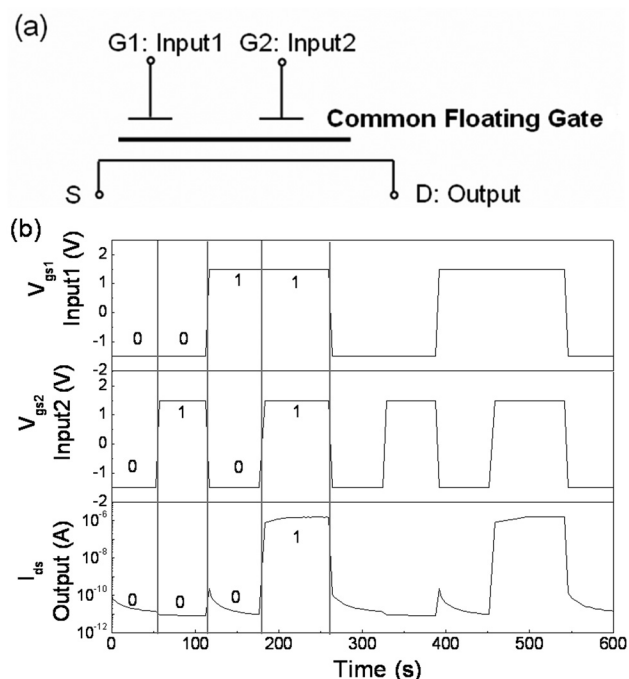


FIG. 6. (a) Logic circuit diagram of the DG neuron TFT. (b) AND logic operation.

technology is highly desirable in terms of the fabrication of high performance neuron transistors with low costs.

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