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Stretchable and Twistable Resistive Switching Memory with Information Storage and Computing Functionalities

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High-performance stretchable and twistable nonvolatile memory devices with logic-in-memory functionality are highly desired for the development of future wearable electronics such as smart clothing. However, it is challenging to fabricate these memory devices using rigid functional materials based on conventional film deposition and patterning techniques. Herein, the first intrinsically stretchable and twistable resistive switching memory is reported using spin-coated poly(dimethyl siloxane) elastomer as the storage medium and printed liquid metal as the electrodes. The memory device is found to exhibit a reliable resistive switching behavior under up to 30% stretching strain and 90° torsional deformation, possessing a large memory window (≈10^2) and an excellent retention (>10^4 s). Under 30% strain, stretching–release endurance of >500 cycles as well as excellent data integrity during the dynamic stretching–release process is demonstrated. Beyond data storage, logic-in-memory computation prototype represented by a one-bit full adder is successfully implemented within four operation steps based on three stretched memory cells. This work will be highly valuable in materials and structure design towards the development of high-performance and multi-functional wearable electronic modules and systems.

1. Introduction

Wearable electronics like smart clothing is the foundation of Internet of Things, artificial intelligence, and human–machine interaction technologies, which show great potential in changing our future lifestyles in health care, entertainment, communication, etc.[1–5] To advance the development of smart clothing, all functional circuit elements including information storage devices should be stretchable and twistable to ensure not only the integrity of the stored information but also conformal contact with complex curved surfaces during mechanical deformation.[6–8] Taking consideration of both the conventional silicon memory cells and the newly invented information storage technologies, resistive switching memory (also known as resistive random access memory or RRAM in short) can be rationally marked as the most promising stretchable information storage technology due to the structural simplicity of a resistor and the prodigious range of materials selection, in addition to the performance merits of high speed, low power, and intrinsic nonvolatility.[9–15] Moreover, the logic-in-memory functionality of resistive switching memory enables data computation directly in the memory array,[16,17] thus holding the great potential to simplify the circuit architecture and reduce the energy consumption of the entire wearable electronic system.

Structural engineering has often been used to build stretchable resistive switching memories for smart clothing applications. For instance, through embedding rigid memory islands into an elastic substrate, Liu et al. successfully made a resistive switching memory capable of tolerating 50% tensile strain.[18] A stretchable resistive switching memory was also made by Chiang et al. with the pre-strained method, that is, depositing rigid memory cells onto a pre-strained elastic substrate and then releasing the whole structure to obtain stretchability.[19] Nevertheless, these structural engineering-based manufacturing processes are very complex and expensive and thus are unsuitable for high-capacity integration and mass production.[20] Meanwhile, the clear mismatch in terms of elastic modulus between the rigid functional layers and the elastic substrate makes the integrated structure mechanically unstable (such as exfoliation and crack generation) during dynamic stretching, leading readily to device failure.[21,22]

As an alternative method, building resistive switching memories using intrinsically stretchable resistive switching media,

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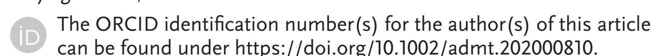
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electrodes, and substrates can address the above questions and can result in stretchable memory devices that are promising in practical applications. As a preliminary attempt, we recently developed an intrinsically stretchable resistive switching memory prototype by integrating the metal–organic framework MIL-53 storage medium and the galinstan@poly(dimethyl siloxane) (GaInSn@PDMS) composite electrode/substrate layer.[22] Despite being functional under stretching, cracking and exfoliation of the MIL-53 layer were observed once the tensile strain reached up to 13%, preventing these devices from being seamlessly accommodated with body parts having a high degree of deformation (such as muscles and joints). Meanwhile, pouring and peeling off processes were included to fabricate the GaInSn@PDMS composite electrode/substrate layer, which is unfavorable for memory array integration. Therefore, to promote the development of smart clothing, it is highly desired to build intrinsically stretchable resistive switching memories with high stretchability through more sophisticated materials selection, structure design, and fabrication procedure optimization. Moreover, implementing data computation functionality based on stretchable resistive switching memories through the logic-in-memory paradigm is also highly desired because low energy consumption is critical for wearable electronic systems.

In this contribution, we report the first intrinsically stretchable and twistable resistive switching memory by spin-coating PDMS elastomer film as the storage medium and printing liquid metal (specifically, Cu microparticles-doped gallium-indium alloy, Cu@GaIn) as the electrodes. During device fabrication, a water-soluble NaCl substrate was used for spin-coating the thin PDMS storage medium film and two thick PDMS encapsulation layers were introduced to support the whole device structure (one for each side). The obtained memory device was found able to exhibit highly reproducible resistive switching behaviors under up to 30% stretching strain and 90° torsional deformation, ensuring at the same time a large memory window of $\approx 10^2$ and a stable data retention of $>10^4$ s. Under the maximum strain of 30%, satisfactory stretching–release endurance of >500 cycles as well as excellent data integrity during the dynamic stretching–release process was demonstrated. Meanwhile, the one-bit full adder function has been successfully implemented within four operation steps based on three stretched memory cells. As such, the fabricated memory device can hold a great potential for application as the information storage and computing components in future wearable electronics like smart clothing. Moreover, by comparison with control devices with various electrode pairs, it is suggested that the printed liquid metal Cu@GaIn electrode not only ensures high conductivity under stretching but also participates in the formation of soft nanofilaments in the PDMS storage medium that accounting for resistive switching.

2. Results and Discussion

The detailed fabrication procedure of our resistive switching memory is distinctly depicted in **Figure 1**. PDMS was used as the dielectric storage medium (PDMS-d) and the encapsulation layers (PDMS-e) due to its good insulating and elastic properties. For the liquid metal Cu@GaIn electrode, it is highly preferred for stretchable electronics applications due to the

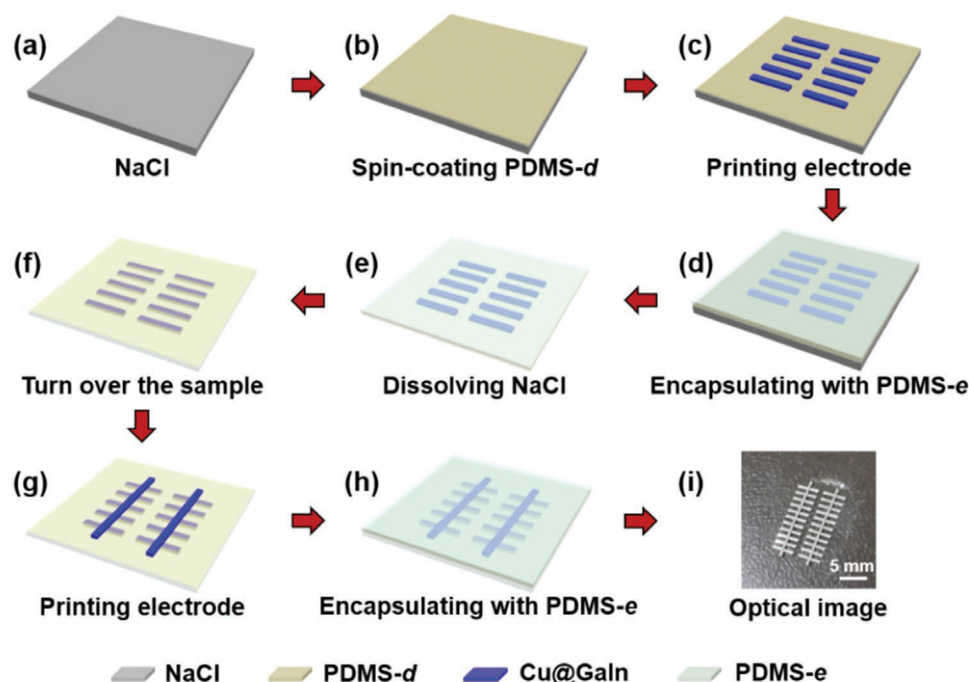

Figure 1. Schematic fabrication procedure of the memory device. a) NaCl substrate. b) Spin-coating the PDMS-d dielectric layer on NaCl substrate. c) Printing multiple parallel Cu@GaIn strip electrodes on PDMS-d layer. d) Encapsulating the sample with a PDMS-e layer. e) Dissolving the NaCl substrate. f) Turning over the sample. g) Printing the single Cu@GaIn strip electrode. h) Encapsulating the sample with another PDMS-e layer. i) Optical image of the fabricated memory device.

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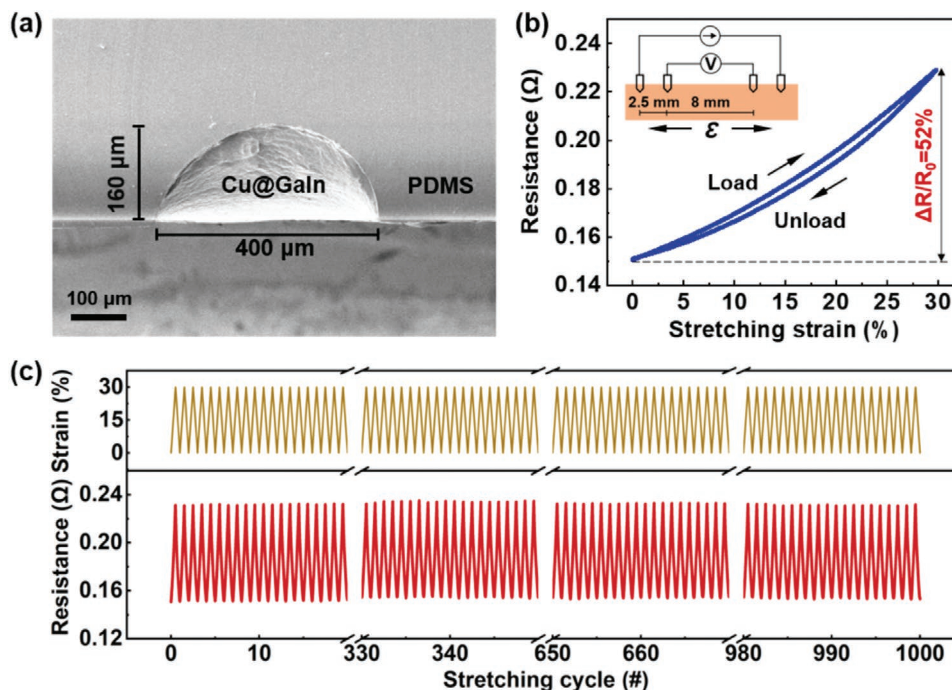

Figure 2. Characterization of the printed Cu@GaIn strip electrode. a) Cross-sectional scanning electron microscope (SEM) image of the electrode. b) Resistance variation of the electrode as the function of strain during a single stretching cycle. The inset shows the schematic test configuration. c) Resistance evolution of the electrode under repeated stretching cycles.

merits of room-temperature fluidity and high electrical conductivity.[23–26] It is noted herein that the inclusion of a small amount of Cu microparticles (specifically, 3.5 wt%) is mainly to reduce the surface energy of pure liquid metal (GaIn:Ga, 75 wt%; In, 25 wt%) for printing fabrication and has little influence on its fluidity and electrical conductivity.[27–29] Six main steps are necessary to fabricate such a memory device, that is, spin-coating the PDMS-d layer on a NaCl substrate (Figure 1b), printing multiple parallel Cu@GaIn strip electrodes on PDMS-d (Figure 1c), encapsulating the sample with a PDMS-e layer (Figure 1d), dissolving the NaCl substrate and turning over the sample (Figure 1e,f), printing the single Cu@GaIn strip electrode (Figure 1g), and encapsulating the sample with another PDMS-e layer (Figure 1h). The thickness of the PDMS-d layer was optimized to be ≈600 nm using the PDMS solution of 95 g L^{-1} to avoid electric leakage and simultaneously to enable lower operation voltages and better switching stability (Figures S1 and S2a, Supporting Information). Also, this layer was found to have a smooth surface with the roughness of only 1.67 nm (Figure S2b, Supporting Information). For the PDMS-e layer, its thickness is ≈0.5 mm, thus making the whole device structure to be ≈1 mm in thickness. An optical image of the fabricated Cu@GaIn/PDMS-d/Cu@GaIn resistive switching memory is provided in Figure 1i. More details about the device fabrication procedure can be found in the Experimental Section.

Characteristics of the printed liquid metal Cu@GaIn strip electrode were carefully examined first. The cross-sectional image of the electrode illustrated in **Figure 2**a suggests that the electrode has an arciform with a width of 400 µm and a height of 170 µm, making the Cu@GaIn/PDMS-d/Cu@GaIn memory cell size to be 400 × 400 μm^2. To evaluate its electrical conductivity especially under dynamic stretching, the standard four-terminal method was used for resistance measurement when the electrode was dynamically stretched and released within 30% strain along the strip direction. Such strain region is normally considered to be enough for most wearable electronics characterizations because the maximum stretching deformation of human skin is 20–30%. The obtained data in Figure 2b indicate that the resistance of an 8 mm long electrode strip increases from ≈0.15 to ≈0.23 Ω upon loading the 30% tensile strain, corresponding a resistance variation of ≈52%. Once unloaded, the resistance can recover to its initial value with negligible hysteresis. Figure 2c exhibits the evolution of the electrode resistance during 1000 consecutive loading and unloading cycles under 30% tensile strain, showing consistent resistance evolution behaviors. These results demonstrate that the printed liquid metal Cu@GaIn strip electrode has both good conductivity and high stretching endurance, allowing it to serve as a promising electrode for stretchable resistive switching memories. Herein, one may doubt whether the relatively high variation of ≈52% in electrode resistance has some influence on stretchable memory operation through the well-known voltage divider effect. Such doubt can be definitely cleared up because the measured electrode resistance even at 30% tensile strain is at least two orders of magnitude smaller than the ON state resistance of normal resistive switching memories (that is, tens to hundreds of ohms).

Now we start to examine the basic resistive switching performance of the Cu@GaIn/PDMS-d/Cu@GaIn memory device without mechanical deformation. During all electrical measurements, the external voltage was applied onto the top Cu@GaIn electrode with the bottom one grounded. **Figure 3**a shows

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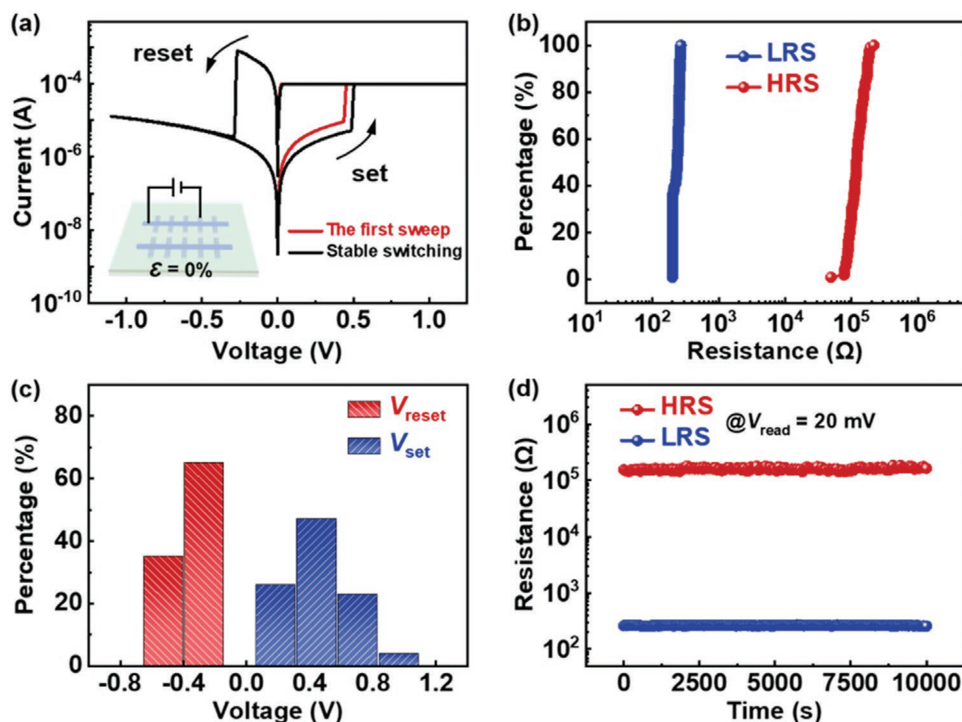

Figure 3. Resistive switching performance of the unstretched memory device. a) Typical I–V curves of the device. The inset shows the schematic measurement configuration. b) Cumulative probabilities of the LRS and HRS resistances. c) Histogram distributions of the V_{set} and V_{reset}. d) Data retention property of the device.

a typical current–voltage (I–V) curve of the memory device during resistive switching. The transition from the high resistance state (HRS or off state) to the low resistance state (LRS or on state), i.e., set process, was triggered at ≈0.5 V during a positive voltage sweep with a compliance current of 0.1 mA to prevent the device from being electrically damaged. Subsequently, to reset the device back into the HRS, a negative voltage sweep was necessary and the transition occurred at ≈–0.3 V, thus giving rise to a bipolar resistive switching behavior in the present memory device. Such a behavior can be repeated for over 100 times (Figure S1c, Supporting Information) and statistical analysis has been made on device resistances and critical voltages to evaluate the switching reliability. As shown in Figure 3b, both the LRS and HRS resistances are distributed in a narrow range, thus guaranteeing a high memory window of >100 that can promise a low misreading probability in practical applications. The histogram in Figure 3c indicates that the set voltage (V_{set}) distributes between 0.1 and 1.1 V, whereas the reset voltage (V_{reset}) ranges from –0.6 to –0.2 V. The device-to-device variations of resistive switching parameters are provided in Figure S3, Supporting Information, which reveals an acceptable device-to-device uniformity. As for data retention property, no degradation in both LRS and HRS resistances can be found within 10^4 s at room temperature (Figure 3d). Based on these results, we conclude that the Cu@GaIn/PDMS-d/Cu@GaIn memory device shows a bipolar resistive switching behavior with good reliability, repeatability, and nonvolatility when no mechanical deformation is applied. Moreover, it is worth mentioning that no apparent electroforming process was needed to activate such resistive switching behavior, as demonstrated by the similar V_{set} value for the first voltage sweep and the stable switching cycle in Figure 3a. This is good for simplifying peripheral circuit of the memory chips and reducing power consumption of the entire integrated circuits in practical applications.

For the involved resistive switching mechanism, it is supposed to be the reversible formation and annihilation of Ga nanofilaments in the PDMS-d layer based on the following reasons. First, substituting the Cu@GaIn electrode by a well-known electrochemically inert Au electrode has been found to make the resistive switching behavior missing (Figure S4b, Supporting Information), demonstrating that the Cu@GaIn electrode is indispensable for resistive switching operation in the present device. Next, the contribution of Cu element to nanofilaments can be reasonably ruled out due to its very small mass percentage of only 3.5% in the Cu@GaIn electrode and the missing of resistive switching behavior after substituting the Cu@GaIn electrode by a pure Cu electrode (Figure S4c, Supporting Information). Finally, the standard electrode potential of Ga/Ga^{3+} (–0.549 V) is more negative than that of In/In^{3+} (–0.3382), making Ga atoms to be more easily oxidized than In atoms under an electric field. Schematic formation and annihilation processes of Ga nano filaments during resistive switching are provided in Figure S5, Supporting Information. In brief, the initial device is in the HRS due to the absence of any filaments in it. When a positive voltage is applied to the top electrode, ionization of Ga atoms into Ga^{3+} cations occurs through Ga → Ga^{3+} + $3e^{-}$. Then, driven by the applied electric field, the generated Ga^{3+} cations will migrate across PDMS-d layer and become reduced by electrons once reaching the

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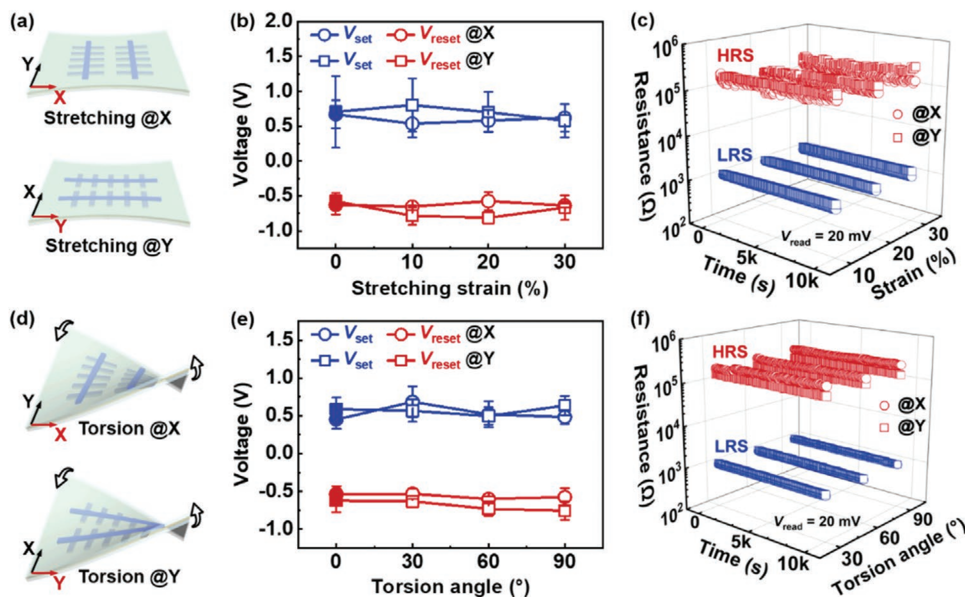

Figure 4. Resistive switching performance of the deformed memory device. a,d) Schematic diagrams of the device when being stretched and twisted along the orthogonal *X* and *Y* directions. b,e) Evolutions of V_{set} and V_{reset} as the function of tensile strain and torsion angle. c,f) Data retention properties of the device under various tensile strains and torsion angles.

bottom electrode, i.e., $Ga^{3+} + 3e^- \rightarrow Ga$. As time goes by, more Ga atoms are deposited onto the bottom electrode and the Ga nano filaments start to nucleate therein and then grow towards the top electrode. Once the filaments are long enough to connect the top and bottom electrodes, the device will be set into the LRS. Subsequently, a negative voltage will annihilate the existing filaments, thus resetting the device back into the HRS. As such, the Cu@GaIn electrodes are considered to not only provide high conductivity but also participate in the resistive switching process.

To evaluate its feasibility for wearable electronics applications, resistive switching performance of the Cu@GaIn/PDMS-d/Cu@GaIn memory device has been carefully characterized under various tensile strains. As shown in **Figure 4**a, the directions along the multiple parallel strip electrodes and the single strip electrode are defined respectively as the orthogonal *X* and *Y* directions for denoting mechanical deformation. The measured evolutions of critical voltages of the device with tensile strain along the two directions are provided in Figure 4b. One can see little degradation in both V_{set} and V_{reset} as the device is stretched along either direction within 30% strain. Similar trends can be found for both LRS and HRS resistances of the device (Figure S6a, Supporting Information). Meanwhile, both LRS and HRS resistances can remain almost unchanged for at least 10^4 s as the device is stretched along either direction within 30% strain, as confirmed in Figure 4c. Moreover, even at the maximum strain of 30%, the device can be consecutively switched for more than 25 cycles with the high memory window of ≈100 (Figure S7, Supporting Information). It is noted that the stretching strain in any direction can be resolved into two component strains along the orthogonal *X* and *Y* directions. Therefore, we can reasonably conclude that the Cu@GaIn/PDMS-d/Cu@GaIn memory device can well retain its resistive switching behavior under stretching along any direction within 30% strain.

Besides stretching, torsion is another common type of mechanical deformation in wearable electronics applications. As such, resistive switching performance of the Cu@GaIn/PDMS-d/Cu@GaIn memory device has also been carefully measured under various torsional deformations (Figure 4d). The obtained results in Figure 4e and Figure S6b, Supporting Information, indicate that both critical voltages and device resistances can remain almost unchanged when the device is twisted from 0° to 90° with the torque direction along either *X* or *Y* axis. Also, data retention property of the device is found to be unaffected by such torsional deformations, as confirmed in Figure 4f. These results can definitely demonstrate a high reliability for the Cu@GaIn/PDMS-d/Cu@GaIn memory device under normal torsional deformations in smart clothing applications.

Fatigue resistance and data integrity under consecutive stretching are also important metrics of stretchable electronic devices. Since there is no essential difference between the *X* and *Y* stretching directions for the Cu@GaIn/PDMS-d/Cu@GaIn memory device, we randomly chose the *Y* stretching direction for such tests. **Figure 5**a schematically shows one complete stretching–release cycle of the device along the *Y* direction with the maximum strain of 30%. For the fatigue resistance test, a total of 500 stretching–release cycles were applied to the device, and statistical analyses were made on both device resistances and critical voltages every 125 cycles. The obtained results in Figure 5b,c indicate that not only the LRS and HRS resistances but also the V_{set} and V_{reset} can remain almost unchanged during the whole test. It is thus concluded that the device can well retain its resistive switching behavior even after 500 stretching–release cycles with the maximum strain of 30%. For the data integrity test, both LRS and HRS resistances of the device were continuously read when it underwent consecutive 500 stretching–release cycles. One can see from Figure 5d that the data written into the device can be well stored during

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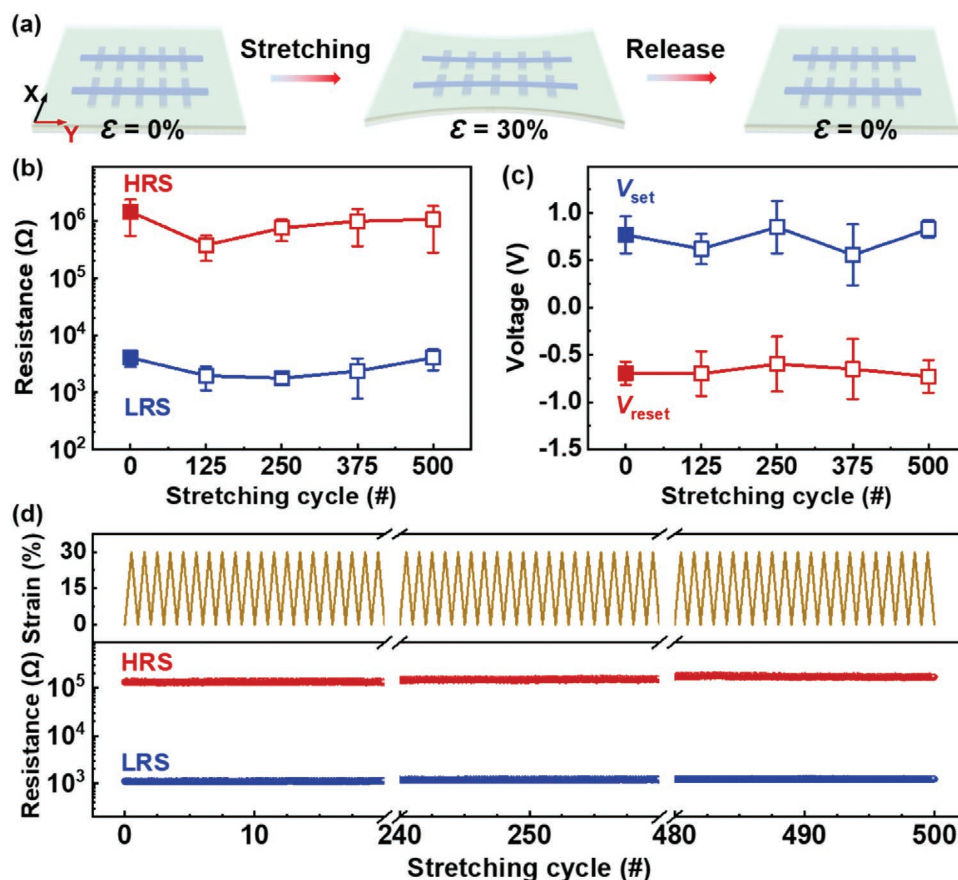

Figure 5. Fatigue resistance and data integrity of the device under consecutive stretching. a) Schematic diagram of a complete stretching–release cycle. b,c) Evolutions of the resistances and programming voltages of the device as the function of stretching–release cycle. d) Data retention property of the device under repeated stretching–release operations.

500 dynamic stretching–release cycles with the maximum strain of 30%. Herein, one may doubt why solid Ga nano filaments in the device can retain intact under dynamic stretching strain. Previous work has proved that ≈10 nm Ag nanoparticles can be pseudoelastic even at room temperature, that is, deforming like a liquid droplet under external stress.[30] Since the melting point of pure Ga is only 29.8 °C, which is much smaller than that of pure Ag (≈962 °C), better pseudoelasticity can be expected in Ga nanomaterials. As such, the observed high data integrity under dynamic stretching is acceptable. Moreover, stable data retention of over 10^4 s can still be confirmed in the device after 500 stretching–release cycles (Figure S8, Supporting Information). These results together demonstrate that the Cu@GaIn/PDMS-d/Cu@GaIn memory device not only has good fatigue resistance for consecutive stretching but also exhibits high data integrity under dynamic stretching, thus promising it a wide application for data storage in smart clothing.

Beyond information storage, the stretchable Cu@GaIn/PDMS-d/Cu@GaIn memory device with reliable nonvolatile resistive switching effects is further explored for in-memory computing applications. Herein, one-bit full adder based on the majority-inverter graph (MIG) logic is employed for the demonstration as it requires less memory cells and operation steps than its counterparts based on other logic paradigms,[31,32] which is beneficial for practical applications especially in wearable electronics where low energy consumption is critical. The MIG logic can be implemented by a single bipolar resistive switching memory cell through one step operation with three input signals and one output signal, as shown in **Figure 6**a. Specifically, input signals of P and Q represent respectively the voltage potentials applied to the top and bottom electrodes (V_t and V_b), whereas input signal R_i and output signal R_o are linked respectively to the original device resistance state and the new device resistance state after logic operation. Assuming that high and low voltage potentials are denoted respectively by logic "1" and "0," the combinations of (P = 1, Q = 0), (P = 0, Q = 1), and (P = Q = 1 or 0) will correspond respectively to the applications of V_{set}, V_{reset}, and V_{cond} (a small voltage that does not affect the resistance state) to the memory cell. With the further assumption that LRS and HRS of the memory device are denoted respectively by logic "1" and "0," the MIG logic can be expressed by $R_o = R(P, Q, R_i) = P(\neg Q) + PR_i + (\neg Q)R_i$, where the symbol "¬" represent the function of inverting (that is, $\neg 0 = 1$ and $\neg 1 = 0$). The truth table of the MIG logic is shown in Figure 6b. Experimental demonstration of the MIG logic based on a single Cu@GaIn/PDMS-d/Cu@GaIn memory cell under 30% stretching strain is provided in Figure S9, Supporting Information, where V_{set} = 1.5 V, V_{reset} = –1 V, V_{cond} = 0 V, LRS resistance is lower than 10^4 Ω, and HRS resistance is higher than that value.

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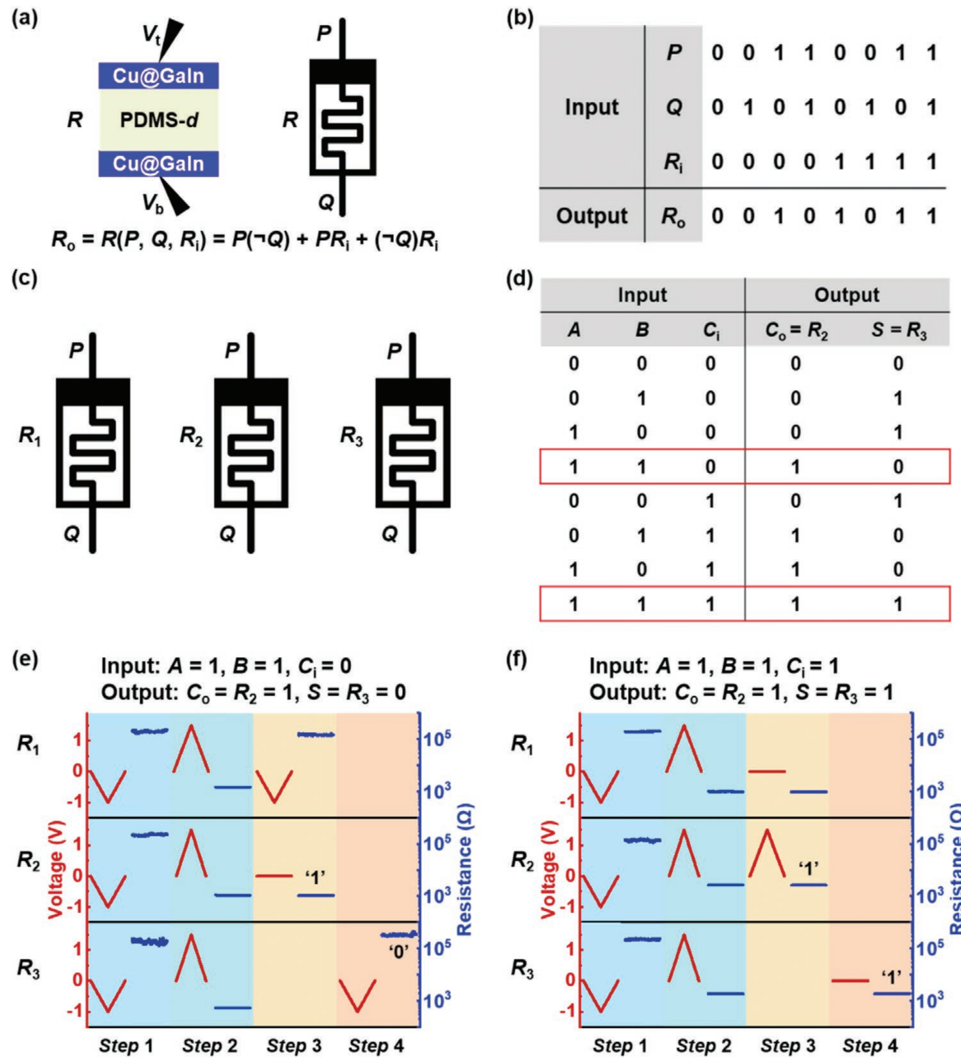

Input			Output	
A	B	C_i	$C_o = R_2$	$S = R_3$
0	0	0	0	0
0	1	0	0	1
1	0	0	0	1
1	1	0	1	0
0	0	1	0	1
0	1	1	1	0
1	0	1	1	0
1	1	1	1	1

Figure 6. The feasibility of data computing in the stretched memory device. a,b) The operation mechanism and truth table of the MIG logic. c,d) The need of three stretched memory cells to perform the MIG logic-based one-bit full adder function and its truth table. e,f) Experimental demonstrations of the one-bit full adder function. The logic operations were implemented by DC voltage sweeps with the operation period of ≈12 s.

Based on the successful demonstration of the MIG logic, the one-bit full adder function can thus be implemented using three Cu@GaIn/PDMS-d/Cu@GaIn memory cells (R_1, R_2, R_3 in Figure 6c) under 30% stretching strain through the following four steps:[32]

Step 1: $R_1(P) = R_2(P) = R_3(P) = 0$, $R_1(Q) = R_2(Q) = R_3(Q) = 1$; $//R_1 = R_2 = R_3 = 0$
Step 2: $R_1(P) = R_2(P) = B$, $R_1(Q) = R_2(Q) = 0$, $R_3(P) = A$, $R_3(Q) = 0$; $//R_1 = R_2 = B$; $R_3 = A$
Step 3: $R_1(P) = C_i$, $R_1(Q) = A$, $R_2(P) = C_i$, $R_2(Q) = \neg A$; $//C_o = R_2$
Step 4: $R_3(P) = R_1$, $R_3(Q) = R_2$; $//S = R_3$

where A, B, C_i, C_o, and S represent the augend, addend, low carry, high carry, and sum of the adder, respectively. The truth table of the one-bit full adder with three input signals (A, B, C_i) and two output signals (C_o, S) is shown in Figure 6d. Experimental demonstrations of the one-bit full adder for ($A = 1$, $B = 1$, $C_i = 0$) and ($A = 1$, $B = 1$, $C_i = 1$) are presented in Figure 6e,f, respectively. Herein, we take ($A = 1$, $B = 1$, $C_i = 0$) as the example to provide a detailed description. In step 1, all memory cells were initialized into the HRS state by applying V_{reset}, leading to $R_1 = R_2 = R_3 = 0$. Then, in step 2, the addend B were written into R_1 and R_2 by applying V_{set}, and the augend A was written into R_3 also by applying V_{set}, resulting in $R_1 = R_2 = R_3 = 1$. Next, in step 3, R_1 was erased back into logic "0" by applying V_{reset} due to $R_1(P) = C_i = 0$ and $R_1(Q) = A = 1$, but R_2 remained unchanged by applying V_{cond} due to $R_2(P) = C_i = 0$ and $R_2(Q) = \neg A = \neg 1 = 0$. That is, after this step, $R_1 = 0$ and the high carry had be calculated to be $C_o = R_2 = 1$. Finally, in step 4, R_3 was erased back into logic "0" by applying V_{reset} due to $R_3(P) = R_1 = 0$ and $R_3(Q) = R_2 = 1$, that is, the sum had be calculated to be $S = R_3 = 0$. These results can definitely demonstrate the feasibility of performing data computing directly in the stretchable Cu@GaIn/PDMS-d/Cu@GaIn memory device.

Before concluding, an instructive discussion is presented to better understand the current work. The above results have

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undoubtedly demonstrated a great potential of the proof-of-concept Cu@GaIn/PDMS-d/Cu@GaIn memory device for stretchable data storage and computing applications. This can also be supported by the comparable device performance between our devices and previously reported stretchable memory devices based on structural engineering (Table S1, Supporting Information). Nevertheless, the mA-level V_{reset} of our devices means a relatively high energy consumption. At the same time, the resistive switching endurance of ≈100 cycles and the stretching–release endurance of ≈500 cycles could not be enough for application cases with very frequent operation. Moreover, the switching performance of our devices under the fast pulse operation mode is still unknown at the moment. As such, performance optimization will be done for our devices in future by device size reduction, polymer structure design, device interface optimization, fast pulse operation, and so on. In addition, stretchable selectors are also very necessary to be developed for solving the sneak-path issue when integrating stretchable resistive switching memory cells into high-density crossbar arrays in future.

3. Conclusion

In summary, an intrinsically stretchable and twistable resistive switching memory was successfully fabricated with the core structure of Cu@GaIn/PDMS-d/Cu@GaIn multilayer. The printed liquid metal Cu@GaIn electrode with a high conductivity under stretching can form soft nano filaments in the PDMS-d storage medium that results in reliable resistive switching effect. Under up to 30% stretching strain and 90° torsional deformation, the device shows a typical bipolar resistive switching behavior with high memory window of $\approx 10^2$ and stable data retention of $>10^4$ s. Under the maximum strain of 30%, the device can tolerate no less than 500 stretching–release cycles and the data written into it can be well stored during dynamic stretching. Meanwhile, the one-bit full adder function has been successfully implemented within four operation steps based on three stretched memory cells. This work will thus be very instructive and valuable for constructing high-performance wearable information storage and computing devices, which are essential for developing smart clothing and other wearable intelligent systems in the near future.

4. Experimental Section

Materials Preparation: High-purity metals of Ga (99.99%) and In (99.995%) were purchased from the Beijing Founde Star Science & Technology Co., Ltd. The liquid GaIn alloy was obtained by heating and stirring the mixture of Ga and In with the mass ratio of 75:25 at 80 °C for 45 min. To get the printable Cu@GaIn alloy, the liquid GaIn alloy was then blended with Cu particles (average size: 5 µm) with a mass percentage of 3.5% to the alloy and ground for 40 min. The PDMS (Sylgard 184) was purchased from the Dow Corning Corporation. To make the PDMS-d solution, the as-obtained PDMS was dissolved in hexane with the concentration of 85–100 g L^{-1}, followed by adding the curing agent (Sylgard 184 silicone elastomer curing agent, Dow Corning Corporation) with a mass percentage of 10% to the PDMS and stirring for 5 min. For the PDMS-e solution, it was prepared by directly adding 10% curing agent into the as-obtained PDMS.

Device Fabrication: First, the PDMS solution was spin-coated onto a transparent NaCl substrate (Hefei Kejing Material Technology Co., Ltd.) at 6000 rpm for 45 s and cured at 85 °C for 90 min to obtain the PDMS-d insulating layer. Then, multiple parallel Cu@GaIn strip electrodes with the width of 400 µm were printed onto the PDMS-d layer through a metal shadow mask and encapsulated with a PDMS-e layer, resulting in the multilayer PDMS-e/Cu@GaIn/PDMS-d/NaCl structure. It is noted herein that, to get a better adhesion between the Cu@GaIn electrodes and the PDMS-d layer, a very thin Au layer (≈16 nm) was sputtered before electrode printing. Next, the NaCl substrate was dissolved using deionized water and the remaining freestanding multilayer of PDMS-e/Cu@GaIn/PDMS-d was turned over. Finally, a single Cu@GaIn strip electrode, orienting perpendicularly to the previous multiple parallel ones, was printed onto the PDMS-d layer and encapsulated with a PDMS-e layer as well, leading finally to a $1 \times n$ array of the PDMS-e/Cu@GaIn/PDMS-d/Cu@GaIn/PDMS-e resistive switching memory.

Device Characterization: Cross-sectional samples were examined by a field-emission scanning electron microscope (FESEM, Thermo Scientific, Verios G4 UC). Electric property of the Cu@GaIn strip electrode was obtained using the standard four-point method with a DC current source of Keithley 6221 and a nanovoltmeter of Agilent 3442A. Surface roughness of the PDMS-d layer was evaluated by an atomic force microscope (AFM, Dimension 3100V, Veeco). Resistive switching-related measurements were all conducted using a semiconductor device analyzer (B1500A, Agilent) at room temperature and in atmospheric conditions. External voltages were applied to the single Cu@GaIn strip electrode, with its multiple parallel counterparts grounded all the times. All mechanical deformations were applied by a ball screw linear guide rail stage (Beijing SDCQ Electrical Technology Co., Ltd.). The stretching speed was set to ≈2.6% s^{-1} in the whole work.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

liquid metal, logic-in-memory, resistive switching, stretchable and twistable nonvolatile memory devices

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