# n-type Polycrystalline Si Thick Films Deposited on SiN$_x$-coated Metallurgical Grade Si Substrates

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*Hongliang Zhang, Liqiang Zhu, Liqiang Guo, Yanghui Liu, Qing Wan*[*]

Ningbo Institute of Materials Technology and Engineering, Chinese Academy of Sciences, Ningbo 315201, China

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For photovoltaic applications, low-cost SiN$_x$-coated metallurgical grade silicon (MG-Si) wafers were used as substrates for polycrystalline silicon (poly-Si) thick films deposition at temperatures ranging from 640 to 880 °C by thermal chemical vapor deposition. X-ray diffraction and Raman results indicated that high-quality poly-Si thick films were deposited at 880 °C. To obtain n-type poly-Si, the as-deposited poly-Si films were annealed at 880 °C capped with a phosphosilicate glass. Electrical properties of the n-type poly-Si thick films were investigated by four-probe and Hall measurements. The carrier concentration and electron mobility of the n-type poly-Si film was estimated to be $1.7 \times 10^{19}$ cm$^{-3}$ and 68.1 cm$^2$ V$^{-1}$ s$^{-1}$, respectively. High-quality poly-Si thick films deposited on MG-Si wafers are very promising for photovoltaic applications.

**KEY WORDS: Thermal chemical vapor deposition; Metallurgical grade Si; Polycrystalline silicon (poly-Si) thick films; Phosphorus diffusion**

## 1. Introduction

Polycrystalline silicon (poly-Si) films have attracted attention for more than one decade because of their important applications in high-efficiency solar cells[1] and high-performance thin-film transistors[2,3]. Thermal chemical vapor deposition (CVD) has been proved to be an efficient method for preparing high-quality poly-Si films[4]. Since elevated temperatures ($\geq$800 °C) are needed for high-quality poly-Si deposition, substrates should have a coefficient of thermal expansion (CTE) close to that of Si ($4 \times 10^{-6}$ K$^{-1}$)[5] to avoid peeling off the as-grown silicon layers. Moreover, another important concern is out-diffusion of impurities from the substrate into the active layer during the deposition process for poly-Si deposition at high-temperature. Therefore, only a limited number of substrates are available, such as graphite, mullite, Al$_2$O$_3$, SiN$_x$, SiAlON and Al$_2$O$_3$–SiO$_2$[6–8]. Diffusion barriers such as SiN$_x$ and SiO$_2$ are frequently deposited on these substrates to prevent substrate impurities from contaminating active layers[9–11]. For example, an 85-nm-thick SiN$_x$ layer was used as the diffusion barrier in the prevent of poly-Si films on Al$_2$O$_3$ substrates by aluminum induced crystallization (AIC) method[8]. SiN$_x$-coated metallurgical grade silicon (MG-Si) substrates not only meet the CTE substrate requirements mentioned above, but also possess several advantages over other substrates, such as lower cost and a more mature fabrication process. Moreover, large-scale industrial production is feasible permitting a monolithic integration of MG-Si substrates[12]. However, the applications of the MG-Si substrates for the deposition of poly-Si thick films in photovoltaic applications have not been addressed yet.

Doping is essential to create the photo-active p/n junction. p-type boron treated at 1100 °C using BCl$_3$ as the doping source resulted in a minority carrier lifetime of 0.1–0.2 μs, a carrier concentration of $4.0 \times 10^{17}$ cm$^{-3}$ and a mobility of 69 cm$^2$ V$^{-1}$ s$^{-1}$[13]. n-type doping of as-grown AIC poly-Si films was obtained using a highly phosphorus doped glass solution as the doping source at 1000 °C[8]. Such n-type poly-Si film has a Hall mobility of 25.4 cm$^2$ V$^{-1}$ s$^{-1}$ and an electron concentration of $5.9 \times 10^{20}$ cm$^{-3}$ n-type and p-type doping of the poly-Si films could be achieved at 1100 °C during rapid thermal CVD using phosphosilicate glass (PSG) and borosilicate glass intermediate layers as doping sources, respectively[14]. However, a high-temperature ($\geq$1100 °C) is needed to obtain such p-type or n-type poly-Si films.

In this work, SiN$_x$-coated MG-Si wafers were used as the substrates for high-quality poly-Si thick films deposition. n-type doping was carried out by annealing the as-deposited poly-Si thick films at 880 °C using a PSG layer as the phosphorus source. An electron concentration of $1.7 \times 10^{19}$ cm$^{-3}$ and an electron mobility of 68.1 cm$^2$ V$^{-1}$ s$^{-1}$ were obtained for the n-type poly-Si films.

## 2. Experimental

Fig. 1 shows the schematic diagram to fabricate undoped (Fig. 1(a)) and P-doped poly-Si thick films (Fig. 1(b)). First, a 350 nm-thick $SiN_x$ films were deposited on the MG-Si wafers by plasma enhanced chemical vapor deposition (PECVD) at 400 °C at a pressure of ~30 Pa. The power was fixed at 100 W using a 13.56 MHz RF source. $NH_3$ and $SiH_4$ (90%Ar + 10%$SiH_4$) were supplied into the chamber as reactive gases at a flow rate of 8 and 12 sccm, respectively. Then, the poly-Si thick films were deposited at various deposition temperatures ranging from 640 to 880 °C on these $SiN_x$-coated MG-Si substrates by CVD furnace using $SiH_4$ and $H_2$ at a pressure of 2000 Pa. Rapid, uniform radiant graphite resistance heating elements were used for the sample holder and heater. Doping was carried out at ~880 °C under the background pressure of ~10 Pa. First, the as-deposited poly-Si thick films were put on top of the uniform flat graphite resistance heating elements. Then, PSG coated commercial solar Si wafers with the size of ~2 cm × 2 cm were put on top of the as-deposited poly-Si thick film in a face-to-face mode (Fig 1(b)). No intentional gap is provided between the PSG layer and the poly-Si thick film. At the high-temperature, a large amount of P atoms would out-diffuse from the PSG layer. Thus, the as-deposited poly-Si layer would be doped by the thermally activated P atoms, leading to the formation of the n-type poly-Si layer. For comparison, the poly-Si thick films were also fabricated by a solid-phase crystallization (SPC) process at 1000 °C using amorphous Si (a-Si) thick films deposited at 280 °C by PECVD from $SiH_4$ as the precursor.

The microstructures and the surface morphologies of the poly-Si thick films were analyzed by field emission scanning electron microscopy (FESEM, Hitachi S-4800 operated at accelerating voltage of 4 kV), X-ray diffraction (XRD, Bruker D8 Advance using Cu$K\alpha$ ($\lambda$ = 0.15406 nm) radiation and a thelta−thelta configuration) and Raman spectra (the poly-Si thick films on fused silica substrates) (Renishaw inVia Raman Microscope exited at 488 nm by an argon laser), respectively. Electrical characteristics of the P-doped poly-Si thick films were measured by four-probe (N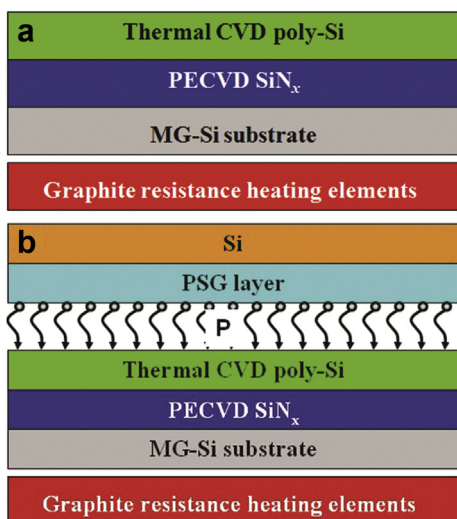APSON CRESBOX) and Hall measurements (Nanometrics HL5500PC). Microwave photoconductivity decay (μ-PCD) mapping was measured with a Semilab (WT-2000PVN) instrument with 904 nm excitation wavelength. Electrochemical capacitance−voltage (ECV) technique (Wafer Profiler CVP21) was used to characterize the doping profile of the n-type poly-Si thick films.

## 3. Results and Discussion

Fig. 2 shows cross-section (a) and top-view (b) SEM images of the poly-Si thick films deposited at 880 °C on the $SiN_x$-coated MG-Si substrate by thermal CVD. The cross-section of the stack films shows that the poly-Si films have a compact morphology with a thickness of up to 20 μm, as shown in Fig. 2(a). The particle size of the poly-Si film increases with increasing film thickness. The thickness of the $SiN_x$ layer is determined to be about 350 nm as shown in the inset of Fig. 2(a). The surface morphologies illustrated in Fig. 2(b) are polycrystalline with an average particle size of up to a few microns.

Fig. 3(a) shows XRD patterns of the thermal chemical vapor deposited poly-Si thick films as a function of deposition temperature. By applying the Scherrer's equation, average crystalline grain sizes of the poly-Si thick films deposited at 640, 800, and 880 °C are calculated to be approximately 31.4, 37.2 and 68.4 nm from (111) peaks, respectively. The dominant crystal orientations are (111) and (220). Fig. 3(b) shows the Raman scattering spectra of the as-deposited poly-Si thick films via thermal CVD at different deposition temperatures. The Raman spectra for poly-Si thick films grown by a solid-phase crystallization (SPC) process and for crystalline Si wafer are also included for comparison. Table 1 summarizes the experimental results obtained from Raman spectra for the poly-Si thick films. It was reported that the spectra can be fitted by one Lorentzian component and two Gaussian components in Raman spectra at around 520, 480 and 500 cm$^{-1}$, respectively, corresponding to
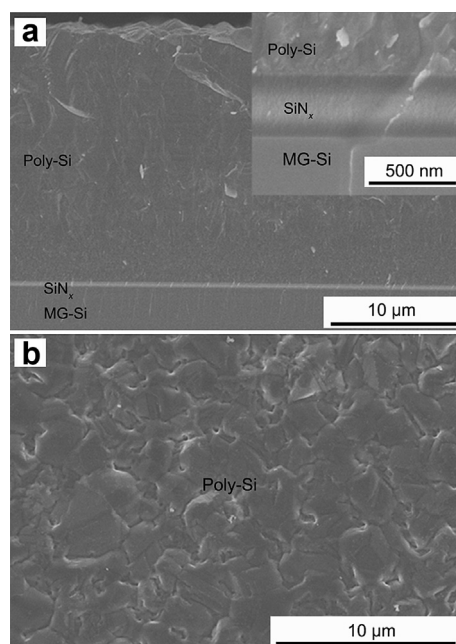


**Fig. 1** Schematic diagram for: (a) depositing poly-Si thick films, (b) obtaining P-doped poly-Si thick films on $SiN_x$-coated MG-Si wafers.



**Fig. 2** Cross-section (a) and top-view (b) SEM images of the poly-Si thick films deposited on $SiN_x$-coated MG-Si wafers. Inset in (a) shows the enlarged cross-section image.
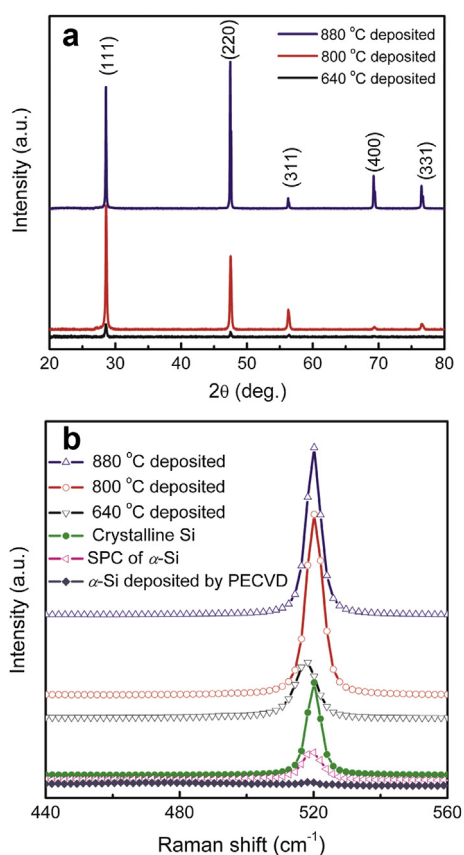
**Fig. 3** (a) XRD patterns of the as-deposited poly-Si thick films as a function of deposition temperature, (b) Raman spectra of the as-deposited poly-Si thick films on fused silica substrate as a function of deposition temperature and the poly-Si thick films grown by SPC.

temperature above 800 °C are completely crystallized, $\chi_C \approx 100\%$. Compared to SPC at 1000 °C, poly-Si thick films grown by thermal CVD at the low temperature of ∼800 °C have a higher crystalline fraction. Hence, the Raman spectra of the poly-Si thick film deposited at temperature above 800 °C are identical to the spectrum of a crystalline Si wafer, as shown in Fig. 3(b). In addition to XRD, Raman scattering can be used for the determination of the mean grain size[16]. The mean grain size $<L>$ can be estimated by the following expression[17]:

$$\Gamma = \Gamma_0 + Q(1/<L>) \tag{1}$$

where $\Gamma_0$ of 0.424 meV represents the intrinsic broadening of c-Si at 520 cm$^{-1}$, and $Q = 1.81$ meV nm with $L$ expressed in nm and $\Gamma$ in meV for $E_2$ structure (in $\Sigma$ direction). The mean grain sizes of the poly-Si thick films deposited at 640, 800 and 880 °C are estimated to be approximately 4.8, 12.5 and 193.2 nm, respectively. It should be noted here that the grain sizes estimated by XRD and Raman are below 0.2 μm, while the observable particle sizes from SEM are up to a few microns. The small grains of synthetic poly-Si are clustered into larger particles during the growth process at high substrate temperature of 880 °C. Though the particles are composed of the poly-Si grain in nano-size, the grain boundary could not be observed by our SEM due to the limited resolutions. Therefore, the observable average width from SEM of the
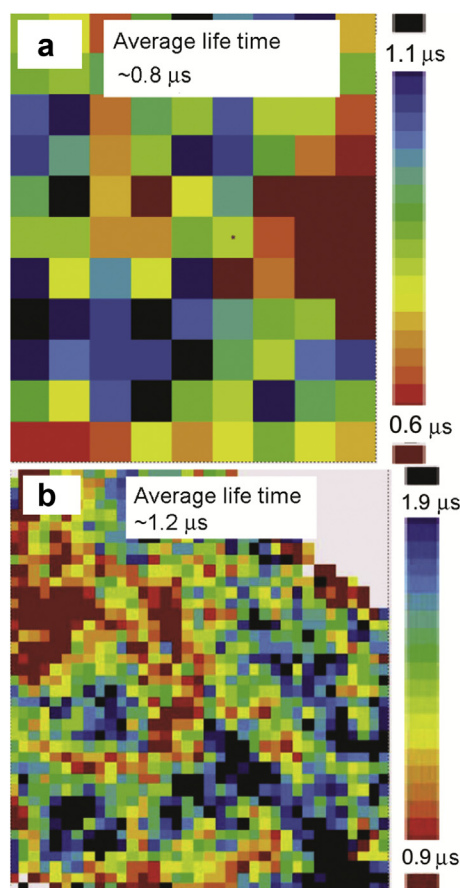
the transverse optical (TO) phonon of crystalline silicon, the TO phonon of amorphous silicon, and the broadening of the 520 cm$^{-1}$ peak due to grain boundaries or a fine crystalline phase in the layer[15]. According to literature[15], the crystalline fraction was estimated as $\chi_C = (A_{520} + A_{500})/(A_{520} + A_{500} + 0.8A_{480})$, where the $A_{520}$, $A_{500}$ and $A_{480}$ are the integrated areas for the three de-convoluted peaks. The crystalline fraction of the poly-Si thick films deposited at 640, 800, and 880 °C are thus estimated to be approximately 98%, 100% and 100%, respectively. For comparison, the crystalline fraction of ∼96% was obtained in SPC grown poly-Si thick film. These results indicate that the poly-Si thick films deposited at

**Table 1** Experimental results obtained from Raman spectra for the poly-Si thick films deposited on fused silica at different temperature of 640, 800 and 880 °C

| Sample | Deposition temperature (°C) | Raman parameter | | Crystallite size (nm) |
|---|---|---|---|---|
| | | ΔΓ | | |
| | | (cm$^{-1}$) | (meV) | |
| 1# | 640 | 3.023 | 0.376 | 4.8 |
| 2# | 800 | 1.076 | 0.134 | 13.5 |
| 3# | 880 | 0.076 | 0.00944 | 193.2 |



**Fig. 4** Minority carrier lifetime mapping of: (a) MG-Si substrates (2 cm × 2 cm), (b) poly-Si thick films (∼30 μm in thickness) deposited on MG-Si wafers (2 cm × 2 cm) with SiN$_x$ barrier layer at 880 °C.

**Table 2**   Sheet resistance of the P-doped poly-Si thick films diffused at 880 °C for 30 min

| Position | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| Ω/Υ | 895.52 | 907.31 | 871.73 | 911.39 | 886.91 | 875.13 | 871.05 | 871.05 |
| Position | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| Ω/Υ | 852.70 | 827.54 | 832.98 | 914.33 | 813.04 | 754.35 | 781.09 | 824.37 |

primary particles may be up to several micron, while the analysis of the X-ray data and Raman data yield a grain size of 0.2 μm or less. In fact, Kamins et al.[18] suggested that the grain size increases as the poly-Si film becomes thicker. The distinct discrepancy of the grain size between Raman or XRD and SEM is due to the increase of the grain size with increasing film thickness. Our results are consistent with their reported results. Based on the above XRD and Raman results, it is concluded that high-quality poly-Si thick films can be obtained by thermal CVD at a temperature of 880 °C.

Fig. 4(a) and (b) show the minority carrier lifetime mapping of the MG-Si substrates and of the poly-Si thick films deposited at 880 °C on MG-Si substrates with SiN$_x$ barrier layer, respectively. The average minority carrier lifetime of the MG-Si wafers is only ~0.8 μs and the maximum minority carrier lifetime is only ~1.1 μs. Moreover, these values are the same as the poly-Si thick film on MG-Si wafers without SiN$_x$ barrier layer. Accordingly, the average minority carrier lifetime of poly-Si

thick films deposited on SiN$_x$ barrier layer coated MG-Si wafers increases to ~1.2 μs and the maximum minority carrier lifetime increases to ~1.9 μs. This indicates that the SiN$_x$ layer plays an important role in hampering the metallic cations contamination in the poly-Si thick film. Thus, the presence of the SiN$_x$, serving as an effective barrier to the diffusion of metallic cations, could be responsible for the increased minority carrier lifetime. The measured lifetime ($\tau_{\text{eff}}$) is an equivalent characteristic of the whole recombination process as described below[19,20]:

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulf}}} + \frac{2S_{\text{eff}}}{W} \tag{2}$$

where $\tau_{\text{bulk}}$, $W$ and $S_{\text{eff}}$ are the bulk carrier lifetime, wafer thickness and surface recombination velocity, respectively. Assuming that both the constant surface recombination level and the bulk carrier lifetime level are constant, the thicker wafer thickness would result in the higher measured lifetime ($\tau_{\text{eff}}$). Therefore, such poly-Si thick films deposited on MG-Si wafers are very promising candidates for photovoltaic applications.

Table 2 lists the sheet resistance of the P-doped poly-Si thick films diffused at 880 °C for 30 min. The sheet resistance of the P-doped poly-Si thick films with the size of ~2 cm × 2 cm determined by four-probe measurements ranges from 911.4 to 754.4 Ω/Υ. Fig. 5 shows the variation of the sheet resistance over a ~2 cm × 2 cm area. An average sheet resistance of ~856 Ω/Υ is obtained. The deviation ($\delta$) is determined to be ~46.8 Ω/Υ using the following formula:

$$\delta = \left( \frac{n \cdot \sum \left( R_{\text{sh}} \right)^2 - \left( \sum R_{\text{sh}} \right)^2}{[n \cdot (n-1)]} \right)^{1/2} \tag{3}$$

where $n$ is the number of measured points. The small deviation value and good sheet resistance uniformity of ~5.47% show the uniform doping. Relatively small wafer size of ~2 cm × 2 cm gives rise to a spatially homogeneous contact
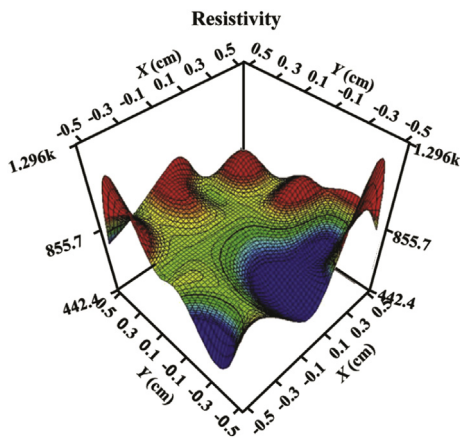


**Fig. 5**   Mapping of sheet resistance for the n-type poly-Si thick film measured on ~2 cm × 2 cm on a SiN$_x$-coated MG-Si substrate. The mapped area is 1 cm × 1 cm.
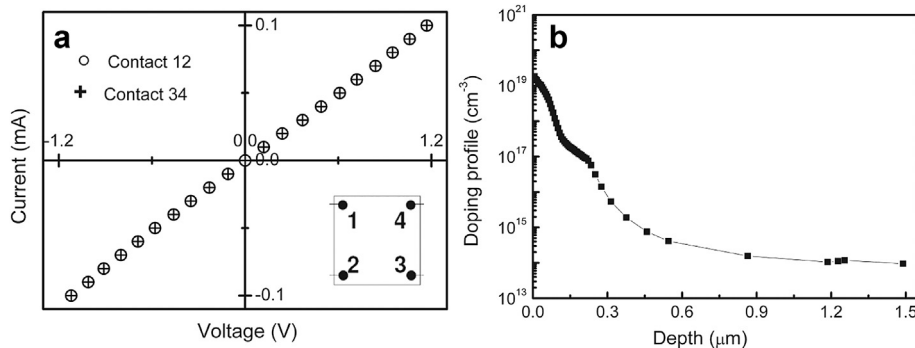


**Fig. 6**   (a) Current−voltage characteristics of the four electrical contacts on the corners of a 1 cm × 1 cm square shaped sample for Van der Pauw configuration, (b) doping profiles measured with the ECV device on the n-type poly-Si thick films grown on a SiN$_x$-coated MG-Si substrate.

and a spatially homogeneous doping profile, because the warpage could be negligible.

Due to the low sheet resistance of $\sim 856$ $\Omega/\Upsilon$ for the P-doped poly-Si thick films, good Ohmic contacts could be obtained by just contacting the sample with the metallic tungsten (W) probes. The linear current−voltage characteristic between probe 1 and probe 2 almost overlaps with that between electrical probe 3 and probe 4, as shown in Fig. 6(a), indicating good doping uniformity. All diffused wafers in this work exhibit n-type characteristic since their Hall coefficients are negative ($-13.3$ $m^2/C$). Sheet resistance, carrier concentration and mobility of the n-type poly-Si films diffused at 880 °C for 30 min are $\sim 737$ $\Omega/\Upsilon$, $\sim 1.7 \times 10^{19}$ $cm^{-3}$ and 68.1 $cm^2$ $V^{-1}$ $s^{-1}$, respectively. The doping profiles have been determined by ECV characterizations as shown in Fig. 6(b). The peak phosphorus concentration is $\sim 1.84 \times 10^{19}$ $cm^{-3}$. The sheet resistance is estimated to be $\sim 653$ $\Omega/\Upsilon$, in good agreement with $\sim 856$ $\Omega/\Upsilon$ obtained from four-probe measurements and $\sim 737$ $\Omega/\Upsilon$ from Hall measurements. In general, the phosphorus doping depth is between 300 and 500 nm for the typical crystalline Si solar cells[21−23]. The phosphorus doping depth of the poly-Si film is much larger than the above values. Considering the microstructures in the poly-Si thick films in our case, two diffusion processes would occur for the P diffusion including at the grain boundary and within the grain. It is believed that impurity diffusion is dominated by grain boundary diffusion for the small grain size[24,25]. Thus, the dominant grain boundary diffusion results in the large minority carrier diffusion length. The results indicate that the doping process is especially needed to be optimized to obtain a good emitter.

## 4. Conclusion

High-quality poly-Si thick films were deposited on $SiN_x$-coated MG-Si wafers by thermal CVD. n-type poly-Si films with an average particle size of up to a few microns were obtained by using the PSG layer as the source. The carrier concentration and mobility of the n-type poly-Si thick films were obtained to be $\sim 1.7 \times 10^{19}$ $cm^{-3}$ and $\sim$ 68.1 $cm^2$ $V^{-1}$ $s^{-1}$, respectively. The average minority carrier lifetime is $\sim 1.2$ μs. High-quality poly-Si thick films deposited on MG-Si wafers offer promising applications in low-cost solar cell.

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