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Proton conducting zeolite films for low-voltage oxide-based electric-double-layer thin-film transistors and logic gates

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Three-dimensional nanoporous zeolite films with Linde Type A (LTA) structure prepared by a seeding-free synthesis strategy exhibited high room-temperature proton conductivity and large electric-double-layer (EDL) capacitance. In-plane-gate indium-zinc-oxide thin-film transistors gated by such proton conducting zeolite LTA films were fabricated by a simple self-assembled method. Due to the strong EDL capacitive coupling triggered by mobile protons in zeolite LTA, such transistors showed a low-voltage operation of 1.5 V and a high performance with a large field-effect mobility of 13 $cm^2\ V^{-1}\ s^{-1}$ and a small subthreshold swing of 95 mV per decade. Furthermore, AND logic operation was also experimentally demonstrated on the dual in-plane-gate EDL transistors. Our results strongly indicate that zeolite LTA films are promising gate dielectric candidates for application in low-voltage and low-cost electronics, which greatly expands the application areas of zeolites.

Introduction

Zeolites are widely used in industry for water purification, as catalysts for the preparation of advanced materials and in nuclear reprocessing due to their uniform three-dimensional (3D) nanoporous structure and high thermal stability.[1–7] Lately, increasing attention has been focused on proton conductivity property in 3D nanoporous zeolite films, as well as the application of zeolite films in proton exchange membrane fuel cells (PEMFCs).[8–10] Among tens of developed zeolite films, zeolite films with Linde Type A (LTA) structure, with a uniform pore size of about 0.4 nm, are of special interest, and show excellent performance in hydrophilic separations.[11,12] Recently, we have developed a seeding-free synthesis strategy for the preparation of high-quality zeolite LTA molecular sieve films for gas separation by using 3-aminopropyltriethoxysilane (APTES) as a covalent linker.[13] The absorbed water molecules in hydrophilic zeolite LTA films can promote proton transfer at the Brønsted acid site by providing a kinetically favorable environment for proton migration, which is favorable for large electric-double-layer capacitance formation. Therefore, zeolite LTA films are promising as gate dielectrics of low-voltage thin-film transistors (TFTs).[14]

Thin-film transistors (TFTs) are the key components of electrical devices.[15] Currently, electric-double-layer (EDL) TFTs, which involve ionic/protonic conductive layered materials as gate dielectrics, have attracted much attention because such gate dielectrics can support very high field-induced charge densities compared with conventional dielectrics.[16–19] The formation of a highly charged EDL with a very thin compact Helmholtz layer greatly enhances capacitive coupling which results in low-voltage operation for TFTs.[20] Up to now, such EDL devices have always been gated by organic based ionic liquids or electrolytes. For example, the Frisbie group have proposed ionic gels or polymer electrolytes as gate dielectrics for low-voltage (below 3 V) organic EDL TFT fabrication.[21,22] There are only limited reports on inorganic oxide based EDL TFTs, which usually endows superior transport properties to organic TFTs.[23] Considering the inherent advantages of semiconducting oxides, it is highly desirable to develop oxide-based EDL devices with a simplified fabrication process. In this work, as shown in Fig. 1(a), three-dimensional nanoporous zeolite LTA films were deposited on ITO glass substrates by a seeding-free synthesis method, and used as the gate dielectric for indium-zinc-oxide (IZO)-based EDL TFT fabrication. A simple one-mask self-assembly process was employed to fabricate dual in-plane-gate EDL TFTs, as shown in Fig. 1(b), and logic operations are experimentally demonstrated.

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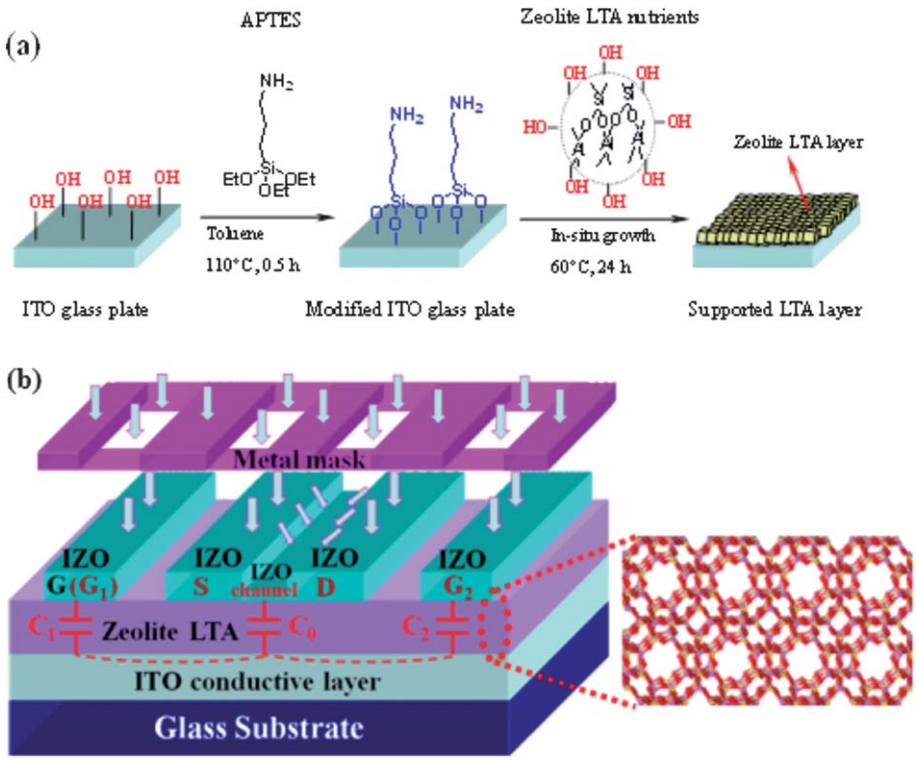

Fig. 1 (a) Schematic diagram of the synthesis of the dense zeolite LTA molecular sieve layer on indium-tin-oxide conductive glass by using APTES as a molecular binder to *in situ* anchor LTA nutrients during hydrothermal synthesis. (b) The self-assembled dual in-plane-gate thin-film transistor by using a zeolite LTA film as the gate dielectric.

Experimental

Synthesis of zeolite LTA films on ITO glass substrates

Zeolite LTA films were synthesized according to our previous procedure.[14,24] Fig. 1(a) illustrates the schematic diagram of the synthesis of the dense zeolite LTA molecular sieve layer on ITO glass substrates by using 3-aminopropyltriethoxysilane (APTES) as a molecular binder to *in situ* anchor LTA nutrients during hydrothermal synthesis. The ITO glass substrates were treated with APTES (0.2 mM in 10 mL toluene) at 110 °C for 1 h under argon, resulting in the APTES coated surface. For the synthesis of zeolite LTA films, a solution with the molar ratio of $Na_2O : Al_2O_3 : SiO_2 : H_2O$ of 50 : 1 : 5 : 1000 was prepared according to the procedure reported elsewhere. Typically, 22.22 g of sodium hydroxide was dissolved in 50 g of deionized water at room temperature, and then 0.30 g of aluminum foil was added to obtain the aluminate solution. The silicate solution was prepared by mixing 4.17 g of LUDOX AS-40 colloidal silica and 47.5 g of deionized water at 333 K under vigorous stirring. The prepared aluminum solution was added into the silicate solution and stirred overnight at room temperature to produce a clear, homogeneous solution. The APTES-functionalized ITO glass substrates were horizontally placed face down in a Teflon-lined stainless steel autoclave which was filled with synthesis solution. After hydrothermal synthesis over 24 h at 60 °C, the solution was decanted off and the film was washed with deionized water several times. Then, the sample was dried in air at 100 °C overnight for characterization.

Fabrication of in-plane-gate EDL TFTs

In-plane-gate EDL TFTs were fabricated on ITO glass substrates with a simple self-assembly process as shown in Fig. 1(b). The fabrication process was performed at room temperature. Source/drain and in-plane-gate electrodes were deposited on zeolite LTA films by radio-frequency (RF) magnetron sputtering with a nickel shadow mask. The IZO film deposition was performed using an IZO target (90 wt% In_2O_3 and 10 wt% ZnO) with a power of 100 W, a working pressure of 0.5 Pa, and an Ar (14 sccm) gas atmosphere. The thin IZO channel layer can be self-assembled between IZO source/drain electrodes during deposition due to the diffraction under the nickel shadow masks. The distance between the nickel mask and the substrate is ~50 μm. The channel length and the channel width are 80 μm and 1000 μm, respectively. For the dual in-plane gate configuration, the distance between G_1 (Gate electrode 1) and the source electrode is 300 μm. The distance between G_2 (Gate electrode 2) and the drain electrode is the same 300 μm.

Electrical characteristics

The measurements of proton conductivity and capacitance behaviors of zeolite LTA films were performed by using a Solartron 1260A impedance analyzer at a relative humidity (RH) of 50%. The measurements of electrical characteristics and logic operations of in-plane-gate EDL TFTs were performed by using a Keithley 4200 semiconductor parameter analyzer in the dark.

Results and discussion

The zeolite LTA films supported on APTES-functionalized ITO glass substrates were prepared according to the procedure reported elsewhere.[24] The microstructure is illustrated by a scanning electron microscope (SEM) image in Fig. 2(a). A uniform and dense zeolite LTA layer was formed on the APTES-functionalized ITO glass substrate. No visible cracks, pinholes or other macroscopic defects are observed in the zeolite LTA layer. The inset in Fig. 2(a) shows the cross-section SEM image of the zeolite LTA layer deposited on a porous aluminum oxide substrate. The thickness of the zeolite LTA layer is found to be ~3.5 μm. A typical X-ray diffraction (XRD) pattern shows a high degree of crystallinity, as shown in Fig. 2(b). All of the peaks match well with those of zeolite LTA, indicating that phase-pure zeolite LTA films with high crystallinity could be formed on the ITO glass surface without seeding.

It is well recognized that the three-dimensional crystalline framework of tetrahedral SiO_4 and AlO_4 structural units creates periodic interconnecting channels and cages in zeolite films.[25]

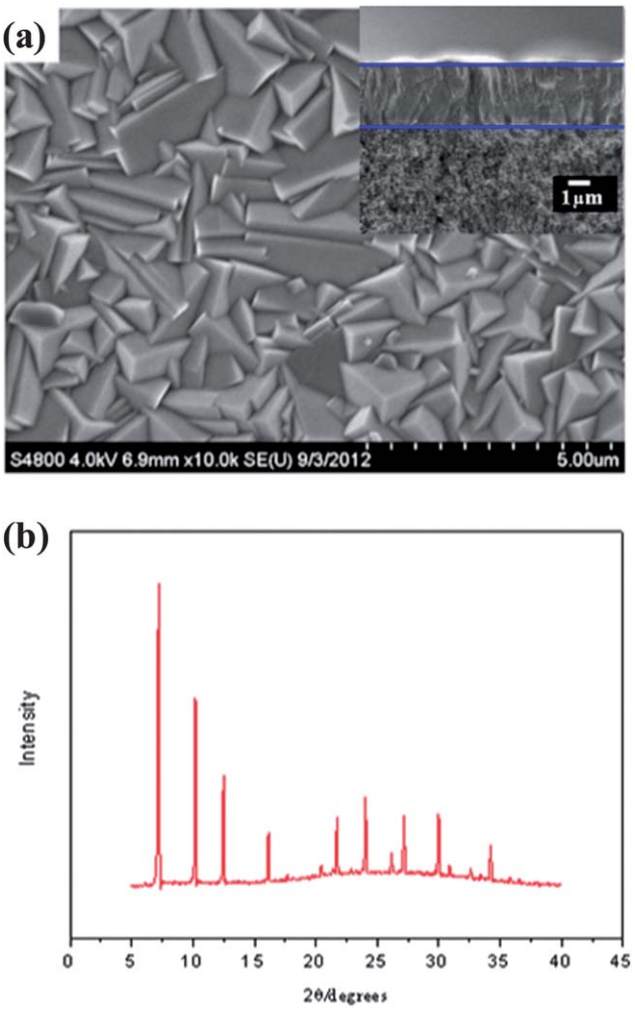

Fig. 2 (a) Top view SEM image of the zeolite LTA film. Inset: cross-section SEM image of the zeolite LTA film deposited on porous Al_2O_3. (b) XRD pattern of the zeolite LTA film.

The insertion of $[AlO_4]^{5-}$ into the $[SiO_4]^{4+}$ framework results in excess negative charges that have to be counterbalanced by positive charges (cations). In the synthesis process of zeolite LTA films, lots of hydroxyl groups were introduced into the surface of the zeolite LTA film and sodium hydroxide was used as one of the reactants. Therefore, the H^+ (protons) and Na^+ are the main positive charge compensation. However, only the protons are movable through the three-dimensional channels, which bridge hydroxyl groups on each Al-site, *i.e.* the so-called Brønsted acid sites.[26] In order to examine the proton conductivity of the as-prepared zeolite LTA film, the Cole–Cole plot was constructed and is shown in Fig. 3(a). The inset is the schematic diagram of the ITO/zeolite LTA/IZO sandwich testing structure. Impedance spectroscopy data are collected as real (Re Z′) and imaginary (Im Z″) components of the complex impedance. The impedance real value (R) of 3000 Ω is obtained with the impedance imaginary value equal to zero. The conductivity (σ) could be obtained from the relation below:[27]

$$\sigma = \frac{D}{(R - R_0)A}$$

where D, A and R_0 are the thickness of the zeolite LTA film, the electrode surface area, and the resistance of the electrodes, respectively. The thickness D is ~3.5 μm, A is ~1.0×10^{-3} cm^2, while R_0 measures ~30 Ω. Therefore, the conductivity (σ) is estimated to be ~1.1×10^{-4} S cm^{-1}, indicating that the zeolite LTA film shows high proton conductivity at room temperature. Fig. 3(b) shows the specific capacitance and phase angle of the zeolite LTA film as a function of frequency in the range between 1.0 Hz and 1.0 M Hz. It can be seen that the specific capacitance

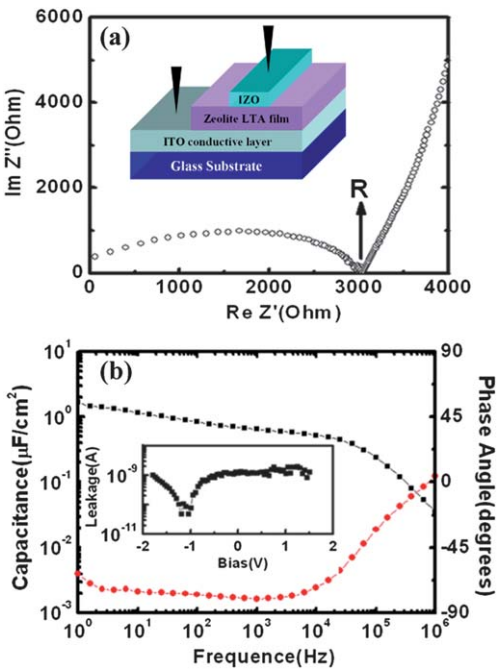

Fig. 3 (a) The Cole–Cole plot of the zeolite LTA film dielectric. Inset: The test structure. (b) The specific capacitance and phase angle of the zeolite LTA film as a function of frequency in the range from 1.0 Hz to 1.0 M Hz. Inset: the gate leakage curve of the zeolite LTA film.

increases with decreasing frequency, and reaches saturation for frequencies below 10 kHz. The specific gate capacitance is ~1.66 μF cm^{-2} at 1.0 Hz. The high capacitance of the zeolite LTA film at low frequency is attributed to its high proton conductivity and the formation of a Helmholtz layer with a thickness of ~1.0 nm at the zeolite LTA/electrode interface. Such behaviors are similar to those of polymer proton conductors.[28] The large specific capacitance can provide a strong capacitive coupling effect between electrons and protons, which can effectively tune the channel conductance at low voltage. In order to further explain the polarization mechanisms of zeolite LTA films, the phase angle was measured as a function of frequency, as also shown in Fig. 3(b). It is well known that the phase angle of an ideal capacitor is −90° while it is 0° for an ideal resistor.[29] Therefore, this phase-angle curve indicates a more resistive behavior at higher frequencies (f > 60 kHz for $\theta(f) < 45°$), and a more capacitive behavior at lower frequencies (f < 60 kHz for $\theta(f) > 45°$). In the high-frequency region (f > 60 kHz for $\theta(f) < 45°$), few protons in the zeolite LTA film could accumulate at the interface due to the inherent limitations for proton mobility. Therefore, ionic relaxation is the dominating polarization mechanism at high frequency. In the low-frequency region (f < 60 kHz for $\theta(f) > 45°$), the EDL formation is the dominating polarization mechanism.[30] In this region, the mobile protons have enough time to migrate from the bulk to the interface. Therefore, the majority of protons in the bulk will drift in response to the electric field, which results in a larger EDL capacitance. Here we should point out that the leakage current of the zeolite LTA film is measured to be <2.0 nA with voltage bias less than 2.0 V, as shown by the inset in Fig. 3(b). The results here strongly indicate that the zeolite LTA film is an electron insulating but proton conducting film and the huge EDL capacitance is favorable for application in low-voltage TFTs as gate dielectrics.

In-plane-gate TFTs gated by such proton conducting zeolite LTA films were fabricated by a simple self-assembly process which has been described in the experimental section. The schematic image of the device is shown in the inset of Fig. 4(a). Output characteristics ($I_{ds} - V_{ds}$) of the TFTs are illustrated in Fig. 4(a). V_{gs} is set from −0.2 V to 0.8 V with 0.2 V steps. The device exhibits an n-type device characteristic with a "hard" saturation at high V_{ds} biases and displays a well-defined linear regime at low V_{ds} biases, which is in good agreement with the standard theory of field-effect transistors. Fig. 4(b) shows the corresponding transfer characteristics at a fixed V_{ds} of 1.5 V. The TFT exhibits high performance with a large current on/off ratio (>10^6) and a small subthreshold swing (SS) of 95 mV per decade. The threshold voltage (V_{th}) estimated from the $(I_{ds})^{1/2}$ *versus* V_{gs} plot was −0.65 V. A small hysteresis window of 0.05 V was observed due to the mobile protons in the zeolite LTA film. The field-effect mobility (μ_{FE}) in the saturation regime ($V_{ds} > V_{gs} - V_{th}$) was estimated to be ~13 cm^2 V^{-1} s^{-1} by the relation $I_{ds} = (\mu_{FE} W C_i / 2L)(V_{gs} - V_{th})^2$, with a channel width ($W$) of 1 mm, a channel length (L) of 80 μm and a specific gate capacitance (C_i) of ~1.66 μF cm^{-2} at 1.0 Hz. To the best of our knowledge, this is the first report of the zeolite LTA film as the gate dielectric in the fabrication of low-voltage oxide TFTs. No photolithography and other complicated defining-pattern processes are involved in the fabrication of in-plane-gate TFTs with self-assembled configurations, which is meaningful for low-cost applications. Further, the transient response of such TFTs was measured by applying a periodic voltage pulse on gate electrodes (not shown). Good reproducibility was obtained and no obvious electrochemical doping occurs at the IZO channel interface when the gate voltage is less than ±1.5 V. The stability remains as one of the crucial issues for practical applications. There are many external environment factors, such as negative or positive gate bias,[31] illumination,[32] temperature[33] and moisture[34] in ambient air, which influence the stability of the TFTs. The effect of these factors on such TFTs will be further investigated in our future work.

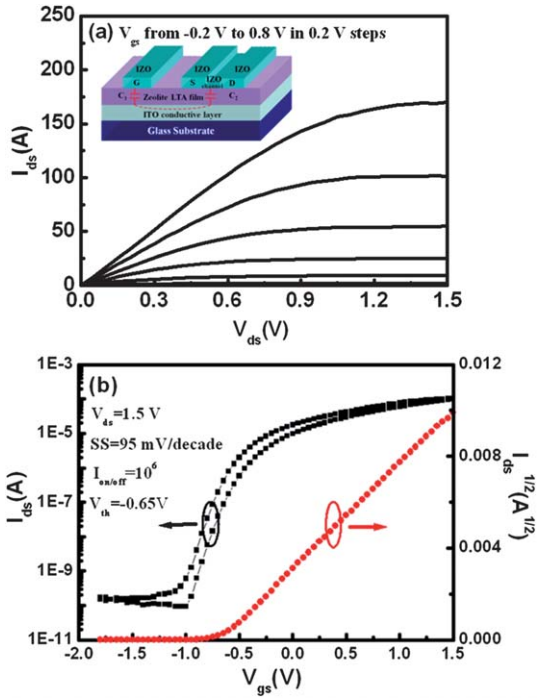

Fig. 4 Electrical characteristics of the in-plane-gate indium-zinc-oxide thin-film transistor gated by the zeolite LTA film. (a) Output characteristics. Inset: The in-plane-gate thin-film transistor structure. (b) Transfer characteristics.

In order to explain the EDL formation and low-voltage operation mechanism of the in-plane-gate EDL TFTs, here, we should point out that the proton migration path is between the oxygen sites neighboring Al,[26] as shown in Fig. 5(a). Moreover, the strong hygroscopicity and moisture retention of the zeolite LTA membrane result in the accumulation of many water molecules in the three-dimensional pore channel, which reduces the energy barrier for proton migration and facilitates proton hopping between the oxygen sites neighboring Al.[35] Therefore, when a negative direct current bias is applied to the gate electrode (marked as G), the proton will move to the gate electrode/zeolite LTA interface, as shown in Fig. 5(b). Because of the existence of the bottom ITO conductive layer, the capacitive coupling between the zeolite LTA dielectric and the channel is in series with C_1 and C_2 connected *via* the bottom ITO conductive layer[36] (see the inset in Fig. 4(a)). As a result, the equivalent negative groups stay near to the zeolite LTA/channel

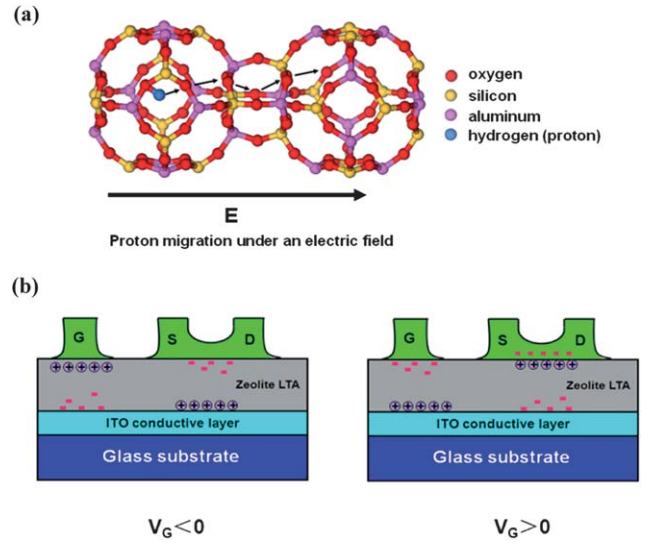

Fig. 5 (a) Schematic diagram of proton migration in zeolite LTA under an electric field. (b) Schematic diagram of electric-double-layer formation and the low-voltage operation mechanism of the in-plane-gate electric-double-layer thin-film transistor.

interface, which depletes the electrons in the channel layer. This is similar to the case of the EDL formation in organic TFTs gated by polyelectrolytes.[37] In contrast, when a positive direct current bias is applied to the gate electrode, protons will move away from the gate electrode/zeolite LTA interface and move to the zeolite LTA dielectric/channel interface, which accumulates the electrons in the channel layer. The changes in proton concentration at the zeolite LTA dielectric/channel interface under gate potential bias result in the variation of currents between the source and the drain, and such behaviors could be also applied in bioelectric devices and in controlling/monitoring the proton variation and conversion between electrical signals and proton signals. Notably, zeolites have various structures, such as LTA, LTL, FAU, and MFI, and the dielectric performance and proton conductivity are structure dependent[38] In our case, zeolite LTA films have high proton conductivity, and they can be gate dielectric candidates for low-voltage EDL TFTs. Proton conducting zeolite films with higher proton conductivity are favorable for faster switch response.[20]

Further, in order to realize logic operation, TFTs with in-plane-gate structure were fabricated by a one-mask self-assembled process, as shown in Fig. 1(b). Fig. 6(a) shows the equivalent logic principle of the dual in-plane-gate TFTs. Different fixed biases applied on two in-plane gates are characterized as Input 1 and Input 2, while the drain currents are regarded as Output. Fig. 6(b) illustrates the logic performance. HIGH input voltage bias (1.5 V) and LOW input voltage bias (−1.5 V) are denoted as state "1" and state ("0"), respectively. The detected HIGH current (>100 μA) and LOW current (<1 nA) are denoted as state "1" and state ("0"), respectively. When both Input 1 and Input 2 are "0", the Output shows "0", while when both Input 1 and Input 2 are "1", the Output shows "1". However, when Input 1 is "1" and Input 2 is "0", or Input 1 is "0" and Input 2 is "1", the Output shows "0". The results indicate that such zeolite LTA

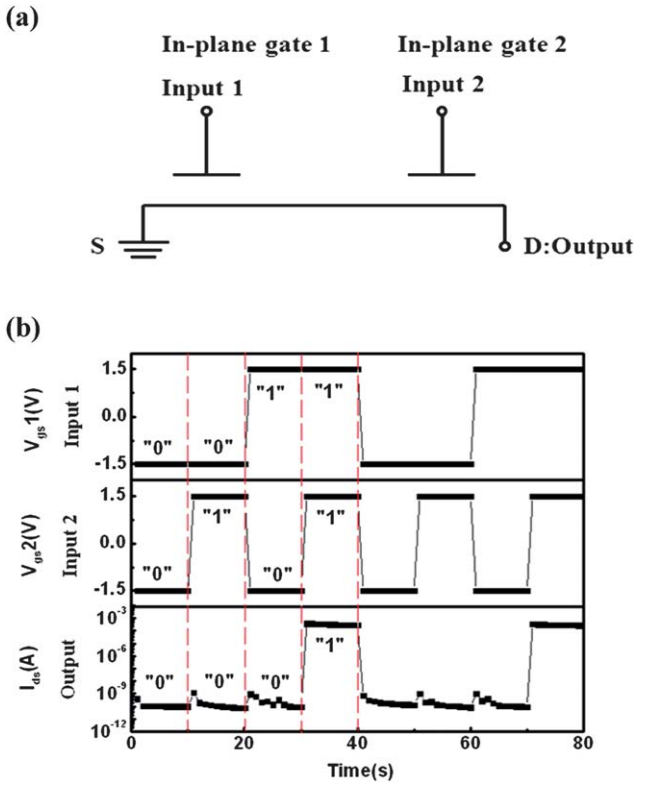

Fig. 6 (a) Logic circuit diagram of the dual in-plane-gate thin-film transistor gated by a zeolite LTA film. (b) Input–output characteristics of the AND logic.

film gated dual in-plane-gate TFTs realize AND logic operation with a high ON/OFF ratio of $>10^5$ at 1.5 V.

Conclusions

In summary, zeolite LTA films prepared by a seeding-free synthesis strategy were used as gate dielectrics for oxide-based EDL thin-film transistors for the first time. Due to the strong electric-double-layer electrostatic coupling effects at the zeolite LTA/IZO channel interface, the device exhibited a low operation voltage of 1.5 V and good electrical performance with a high mobility of >10 $cm^2 V^{-1} s^{-1}$ and a small subthreshold swing of 95 mV per decade. Furthermore, AND logic operation was also demonstrated on such dual in-plane-gate thin-film transistors. Our results demonstrate that zeolite LTA films are promising gate dielectric candidates for application in low-voltage electronics, which greatly expands the application areas of zeolites.

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