In-Plane-Gate Oxide-Based Thin-Film Transistors Self-Aligned on Stacked Self-Assembled Monolayer/SiO$_2$ Electrolyte Dielectrics

Guodong Wu, Hongliang Zhang, Liqiang Zhu, Mingzhi Dai, Ping Cui, and Qing Wan

Abstract—Low-voltage oxide-based thin-film transistors (TFTs) gated by stacked self-assembled octadecylphonic acid (ODPA) monolayer/SiO$_2$ electrolyte with an in-plane-gate structure are self-aligned by one nickel shadow mask at room temperature. The stacked gate dielectrics show a reduced gate leakage current with the aid of the well-organized dense-stacked ODPA monolayer buffer. The equivalent field-effect mobility, subthreshold voltage swing, and drain current on/off ratio of such TFTs are estimated to be 11 cm^2/V·s, 140 mV/dec, and 10^6, respectively. Such low-voltage in-plane-gate TFTs are very promising for low-cost portable sensors.

Index Terms—In-plane gate, monolayer/SiO$_2$ electrolyte, self-assembly.

I. INTRODUCTION

CONVENTIONAL field-effect transistors have a sandwich structure with the gate placed on the top or at the bottom of the channel between source and drain electrodes. In contrast, in-plane-gate transistors are devices with source/drain and gate electrodes located on the same plane. The special features of such devices are simple fabrication process and inherent self-alignment [1]. The source/drain and gate electrodes were defined by several techniques, such as laser-induced diffusion, ion implantation, and trench etching [2]–[4]. Up to now, thin-film transistors (TFTs) with in-plane-gate structure are of little research. The main problems for in-plane-gate TFTs are the weaker capacitive coupling, compared with the conventional field-effect transistors and complicated defining-pattern process. These problems result in large operation voltages and high cost of the fabrication process, which are the major barriers for low-cost portable application.

In order to reduce the operation voltage of the TFTs, several methods were reported to enlarge the specific gate capacitance, such as decreasing the thickness of the gate dielectrics, choosing insulators with high dielectric constant [5]–[7], and using

ion gel or ionic liquid with electric-double-layer (EDL) effect [8], [9]. At the same time, self-assembled monolayers (SAMs) have recently attracted much attention for low-voltage TFTs due to its decreased thickness of several nanometers. SAMs are kinds of ultrathin well-organized dense-stacked films [10], [11]. Lately, our group has reported low-voltage oxide-based TFTs gated by nanoporous SiO$_2$-based electrolytes with a huge EDL capacitance [12]. Such SiO$_2$-based electrolytes give a promising route for low-voltage TFT fabrication. In this letter, we explore stacked octadecylphonic acid (ODPA) monolayer/SiO$_2$ electrolyte as the gate dielectric for low-voltage in-plane-gate oxide-based TFT fabrication. The SiO$_2$ electrolyte provided huge EDL capacitance, and the ODPA monolayer acted as a buffer layer to further reduce the gate leakage. Furthermore, the source/drain, self-aligned channel, and in-plane gate can be deposited simultaneously by using only one nickel shadow mask. Such low-voltage in-plane-gate TFTs are very promising for low-cost portable sensor application.

II. EXPERIMENTAL DETAILS

All processes for device fabrication were performed at room temperature. First, ITO substrates were immersed into a 1.0-mM ethanolic solution of ODPA for 24 h and then thoroughly rinsed with ethanol and dried in a stream of nitrogen. Second, a 400-nm-thick SiO$_2$-based electrolyte film was deposited onto the self-assembled ODPA monolayer covered ITO glass substrate by plasma-enhanced chemical vapor deposition using SiH$_4$ and O$_2$ (3:18) as reactive gases at room temperature. Third, 200-nm-thick ITO films for source/drain and in-plane-gate electrodes were deposited on the stacked gate dielectrics simultaneously by radio-frequency (RF) magnetron sputtering with a nickel shadow masks. ITO films were deposited in 0.5-Pa pure argon ambient with an RF power of 100 W. An thin ITO channel layer can be self-assembled between ITO source/drain electrodes during deposition due to the diffraction under the nickel shadow masks. The distance between nickel mask and substrate is ∼50 μm. The distance between the in-plane gate and the source electrode was 300 μm. For circuit application, the bottom ITO film should be patterned, and it can be patterned by photolithography or laser scribing. Capacitance-frequency curve of the stacked gate dielectrics was measured by a Solartron 1260 impedance analyzer. The electrical characteristics of the devices were measured by a Keithley 4200 semiconductor parameter analyzer at room temperature in the dark.
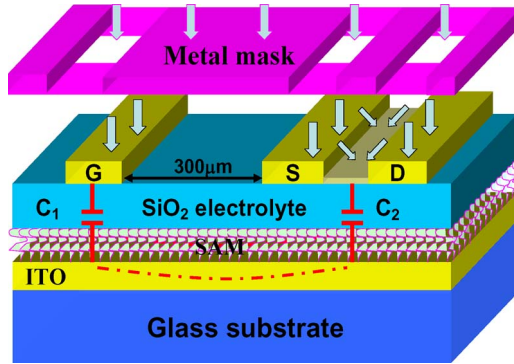
Fig. 1. Schematic diagram of ITO-based TFTs with an in-plane-gate structure self-aligned on stacked SAM /SiO$_2$ electrolyte dielectrics.
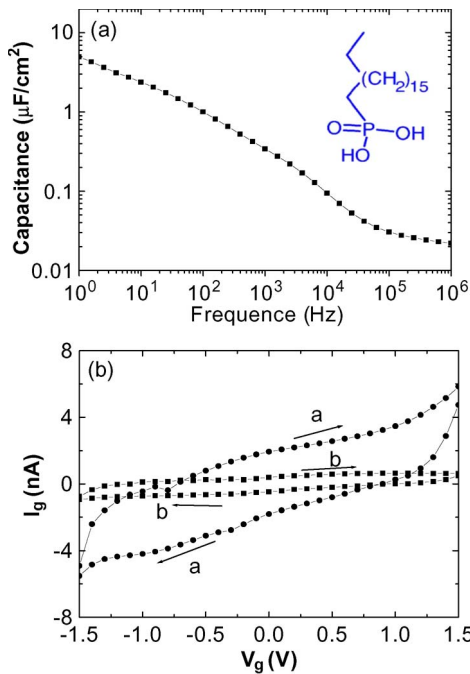

Fig. 2. (a) Frequency-dependent capacitance curve of the stacked gate dielectric film. The inset shows the molecular structure of ODPA. (b) Leakage-voltage curves of two kinds of gate dielectrics. Curve a: 400-nm SiO$_2$-based electrolyte. Curve b: stacked self-assembled ODPA monolayer/SiO$_2$ electrolyte dielectrics.

III. RESULTS AND DISCUSSION

Fig. 1 shows the schematic diagram of the in-plane-gate TFTs self-assembled on stacked ODPA monolayer/SiO$_2$ electrolyte dielectrics. The ITO active channel thickness gradually decreases from the edge of the source/drain electrode to the middle of the self-assembled ITO channel. The thinnest part of the ITO channel is estimated to be 40 nm. Fig. 2(a) shows the specific capacitance of stacked ODPA monolayer/SiO$_2$ electrolyte dielectrics in the frequency range of 1.0 Hz–1 MHz with an ITO/ODPA monolayer/SiO$_2$ electrolyte/ITO sandwich test structure. The specific capacitance increases with decreasing frequency and shows a value of 4.9 μF/cm^2 at 1.0 Hz due to the interfacial EDL effect [12]. The inset in Fig. 2(a) depicts the molecular structure of ODPA. Fig. 2(b) shows the gate leakage curves of the two kinds of gate dielectrics. The area of the tested
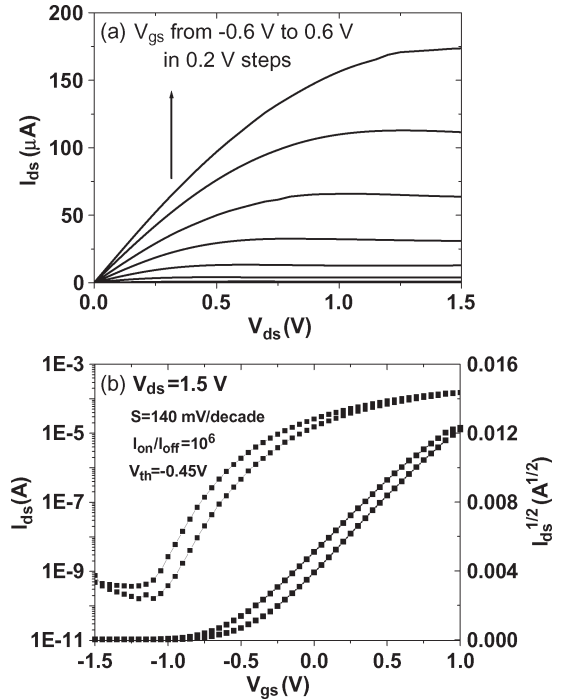

Fig. 3. Electrical characteristics of ITO-based TFTs with in-plane-gate structure. (a) Output characteristics (I_{ds}–V_{ds}). (b) Transfer characteristics ($V_{ds} = 1.5$ V).

region is 1.5×10^{-3} cm^2. SiO$_2$-based electrolyte film shows a leakage current of 6.0 nA at 1.5 V. While the leakage current of ODPA monolayer/SiO$_2$ electrolyte stacked dielectrics was measured to be less than 0.8 nA at 1.5 V, which is almost one order of magnitude lower than that of the single SiO$_2$ electrolyte dielectric. The low leakage current guarantees that the TFT operation would not be affected by the gate leakage.

Here, we give a possible explanation for the operation mechanism of such in-plane-gate TFTs. With a bottom ITO conductive layer, it gives a strong capacitive coupling between the in-plane gate and the active channel. Two capacitors in series (C_1 and C_2) can be used to interpret this model, as shown in Fig. 1. Each one can be described as an equivalent EDL capacitor based on a vertical-stack sandwich structure. C_1 and C_2 are coupled by the bottom ITO film between stacked ODPA monolayer/SiO$_2$ electrolyte gate dielectrics and glass substrate. Without bottom ITO layer, C_1 and C_2 cannot be coupled effectively, and the field-effect is only through lateral direction. The low capacitance in the lateral direction between gate and channel results in a poor device performance.

Fig. 3(a) shows the output characteristics (I_{ds}–V_{ds}) of such TFTs. V_{gs} was varied from -0.6 to 0.6 V in 0.2-V steps. The I_{ds}–V_{ds} curves of such device have well-defined linear regimes at low V_{ds} biases and saturation regimes at high V_{ds} biases, which is in good agreement with the standard theory of field-effect transistors. Fig. 3(b) shows the corresponding transfer characteristics at a fixed $V_{ds} = 1.5$ V. The TFTs exhibit a high performance with a large current on/off ratio (10^6) and a small subthreshold swing of 140 mV/dec. A threshold voltage (V_{th}) of -0.45 V was calculated from the x-axis intercept of the square root of I_{ds}-versus-V_{gs} plot. A small hysteresis
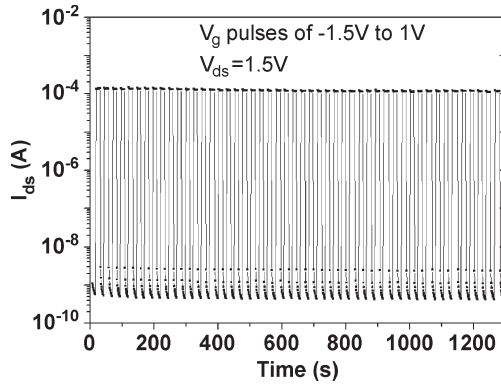
Fig. 4. Transient response of the in-plane-gate TFTs self-assembled on stacked SAM/SiO$_2$ electrolyte dielectrics.

window of ∼0.08 V is observed due to the mobile protons in the SiO$_2$ electrolyte. The field-effect mobility (μ_{FE}) in the saturation regime, which was extracted from the linear fitting of the experimental results to the curve of $I_d^{1/2}$ versus V_g, was estimated to be 11 cm^2/V · s. The field-effect mobility was derived from the following equation:

$$I_{ds} = \left(\frac{\mu_{FE} W C_i}{2L} \right) (V_{gs} - V_{th})^2$$

where $L = 50$ μm is the channel length, and $W = 1000$ μm is the channel width. C_i is the capacitance between gate and source electrode, which, from our proposed in-plane gate structure model, $C_i = C_1 C_2/(C_1 + C_2) = 1/2C_1 = 2.45$ μF/cm^2, because C_1 and C_2 is an equivalent capacitance, $C_1 = C_2$.

The stability measurements of such TFTs were also investigated. Fig. 4 shows the transient response of the in-plane-gate TFTs to a square-shaped V_{gs} with a pulsed amplitude of $V_+ = 1.0$ V and $V_- = -1.5$ V, under a constant bias of $V_{ds} = 1.5$ V. Such TFTs exhibited good reproducibility because the OFF current was almost unchanged and the current on/off ratio nearly kept to be a constant ($> 10^5$). This indicates that ions in the SiO$_2$ electrolyte have not penetrated into the ITO channel and no obvious electrochemical doping occurs at the ITO channel and SiO$_2$ electrolyte interface when the gate potential is biased. Such device is not suitable for high-frequency electronics due to the limitation of EDL dielectric and unnecessary parasitic capacitance related to the in-plane-gate structure, but it is favorable for low-cost portable sensor applications because low switching speed is enough.

IV. Conclusion

In conclusion, low-voltage in-plane-gate ITO-based EDL TFTs gated by ODPA monolayer/SiO$_2$ electrolyte stacked gate dielectrics have been self-aligned on ITO-based conducting glass substrates at room temperature by using only one metal mask. The stacked gate dielectrics have shown a large EDL capacitance and reduced leakage current with the aid of the well-organized dense-stacked ODPA monolayer. The equivalent field-effect mobility, subthreshold swing, and current on/off ratio was estimated to be 11 cm^2/V · s, 140 mV/dec, and 10^6, respectively. Such low-voltage in-plane-gate EDL TFTs processed at room-temperature are very promising for low-cost portable sensor applications.

References

[1] A. D. Wieck and K. Ploog, "In-plane-gated quantum wire transistor fabricated with directly written focused ion beams," *Appl. Phys. Lett.*, vol. 56, no. 10, pp. 928–930, Mar. 1990.

[2] J. Nielder, A. D. Wieck, P. Grambow, H. Lage, D. Heitmann, K. V. Klitzing, and K. Ploog, "One-dimensional lateral-field effect transistor with trench gate-channel insulation," *Appl. Phys. Lett.*, vol. 57, no. 25, pp. 2695–2697, Dec. 1990.

[3] H. Pothier, J. Weis, R. J. Haug, K. V. Klitzing, and K. Ploog, "Realization of an in-plane gate single-electron transistor," *Appl. Phys. Lett.*, vol. 62, no. 24, pp. 3174–3176, Jun. 1993.

[4] J. A. Garrido, C. E. Nebel, R. Todt, G. Rosel, M.-C. Amann, and M. Stutzmann, "Fabrication of in-plane gate transistors on hydrogenated diamond surfaces," *Appl. Phys. Lett.*, vol. 82, no. 6, pp. 988–990, Feb. 2003.

[5] K. D. Kim and C. K. Song, "Low-voltage pentacene thin-film transistors employing a self-grown metal-oxide as a gate dielectric," *Appl. Phys. Lett.*, vol. 88, no. 23, p. 233 508, Jun. 2006.

[6] J. B. Kim, C. Fuentes-Hernandez, W. J. Potscavage, X. H. Zhang, and B. Kippelen, "Low-voltage InGaZnO$_4$ thin-film transistors with Al$_2$O$_3$ gate insulator grown by atomic layer deposition," *Appl. Phys. Lett.*, vol. 94, no. 14, p. 142 107, Apr. 2009.

[7] D. H. Kim, N. G. Cho, H. G. Kim, H. S. Kim, J. M. Hong, and I. D. Kim, "Low-voltage operating InGaZnO$_4$ thin-film transistors using high-k MgO-Ba$_{0.6}$Sr$_{0.4}$TiO$_3$ composite gate dielectric on plastic substrate," *Appl. Phys. Lett.*, vol. 93, no. 3, p. 032 901, Jul. 2008.

[8] S. Ono, S. Seki, R. Hirahara, Y. Tominari, and J. Takeya, "High-mobility, low-power, and fast-switching organic field-effect transistors with ionic liquids," *Appl. Phys. Lett.*, vol. 92, no. 10, p. 103 313, Mar. 2008.

[9] M. J. Panzer and C. D. Frisbie, "Exploiting ionic coupling in electronic devices: Electrolyte-gated organic field-effect transistors," *Adv. Mater.*, vol. 20, no. 16, pp. 3177–3180, Aug. 2008.

[10] D. Vuillaume, C. Boulas, J. Collet, J. V. Davidovits, and F. Rondelez, "Organic insulating films of nanometer thicknesses," *Appl. Phys. Lett.*, vol. 69, no. 11, pp. 1646–1648, Sep. 1996.

[11] P. Thissen, M. Valtiner, and G. Grundmeier, "Stability of phosphonic acid self-assembled monolayers on amorphous and single-crystalline aluminum oxide surfaces in aqueous solution," *Langmuir*, vol. 26, no. 1, pp. 156–164, Jan. 2010.

[12] A. X. Lu, J. Sun, J. Jiang, and Q. Wan, "Microporous SiO$_2$ with huge electric-double-layer capacitance for low-voltage indium tin oxide thin-film transistors," *Appl. Phys. Lett.*, vol. 95, no. 22, p. 222 905, Nov. 2009.