Transparent In-Plane-Gate Junctionless Oxide-Based TFTs Directly Written by Laser Scribing

Liqiang Zhu, Guodong Wu, Jumei Zhou, Hongliang Zhang, and Qing Wan

***Abstract*—A laser-scribing process without any mask and photolithography is developed for transparent junctionless oxide-based in-plane-gate thin-film transistor (TFT) fabrication at room temperature. Such junctionless TFTs feature that the channel and the source/drain electrodes are of the same thin indium–zinc–oxide films. Good electrical performance with an I_{on}/I_{off} ratio of 4×10^5, a field-effect mobility of 15 $cm^2/V \cdot s$, and a subthreshold swing of 0.12 V/dec is obtained. AND logic is realized with a reliable logic operation in a dual in-plane-gate configuration. The developed laser-scribing technology is highly desirable in terms of the low-cost fabrication process.**

***Index Terms*—In-plane-gate thin-film transistors (TFTs), laser scribing.**

I. Introduction

In conventional thin-film transistor (TFT) fabrication, photolithography or shadow mask process is inevitably adopted in order to form a patterned channel layer and source/drain electrodes. Recently, a concept of junctionless transistors has been proposed [1]–[3]. However, the fabrication of such a junctionless device is still rather challenging. Self-assembled patterned channel layers have been achieved by applying only one shadow mask, addressing coplanar junctionless TFTs [4], [5]. A laser-scribing process as a novel technology with low cost was also proposed for source/drain patterning [6], [7]. However, masks are still needed during the TFT fabrication. Therefore, the fabrication of junctionless TFTs with simplified process is particularly needed to be developed.

In this letter, a laser-scribing method without any mask and photolithography is developed to directly write in-plane-gate junctionless indium–zinc–oxide (IZO) TFT arrays on glass substrates at room temperature. Good electrical performance has been exhibited that is to say a low OFF current of < 0.1 nA, an I_{on}/I_{off} ratio of 4×10^5, an electron mobility of 15 $cm^2/V \cdot s$, and a low subthreshold swing of 0.12 V/dec. AND logic is realized with a reliable logic operation in a dual in-plane-gate configuration. The developed laser-scribing technology is highly desirable in terms of the low-cost fabrication process.

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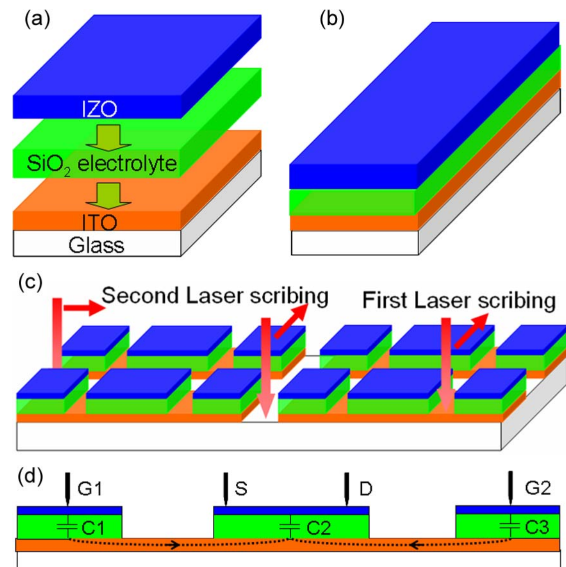

Fig. 1. (a) SiO_2-based solid electrolyte and IZO layers are subsequently deposited onto ITO glass by PECVD and sputtering, respectively. (b) Obtained IZO/SiO_2 electrolyte/ITO/glass stack. (c) Laser-scribing process results in the in-plane-gate TFT arrays. (d) Schematic cross-sectional view of the laser-patterned in-plane-gate junctionless TFTs. The capacitors C1, C2, and C3 are effectively coupled through the bottom conducting ITO films.

II. Experimental Details

IZO-based transparent in-plane-gate junctionless TFTs were fabricated on a transparent conducting ITO glass substrate, as shown in Fig. 1. First, a 2-μm-thick nanogranular SiO_2-based solid electrolyte film was deposited by plasma-enhanced chemical vapor deposition (PECVD) using SiH_4 and O_2 as reactive gases [4], [5]. Then, 37-nm-thick IZO films were deposited on the SiO_2 electrolyte by sputtering. For TFT patterns, a laser-scribing process was adopted at room temperature. The laser wavelength is 532 nm, and the scanning step length is 1.0 μm with a laser-scribing delay time of 200 μs. Since the laser scanning setup is computer controlled, the exact and highly reproducible positioning can be realized. Due to the edge roughness, the minimum feature would be ~100 μm in our case. The creation of an effective localized heating zone by the focused laser beam results in a localized physical or chemical state transition. Therefore, IZO films could be selectively etched out due to a localized thermoelastic force caused by rapid thermal expansion resulting from the pulsed laser irradiation. The first laser-scribing process results in the isolation of the top IZO films, whereas the bottom ITO layer remains continuous. The second scribing process results in the isolation of both top IZO and bottom ITO films. The laser-patterned

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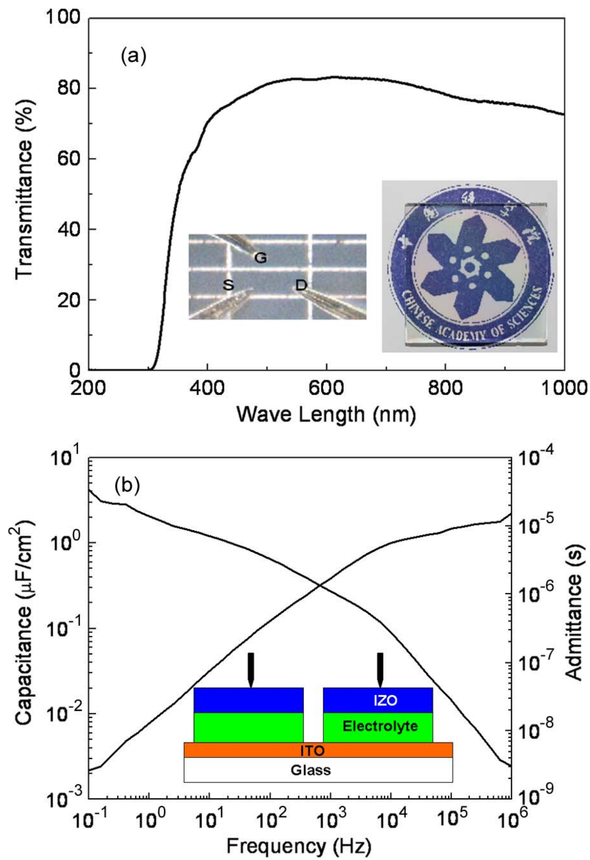

Fig. 2. (a) Optical transmittance spectrum of the laser-scribed IZO-based in-plane-gate junctionless TFT arrays on the glass substrate. (b) Specific gate capacitance and the ionic conductivity of the SiO_2 electrolyte film as a function of frequency. (Inset) IZO/SiO_2-based electrolyte/ITO in-plane test structure.

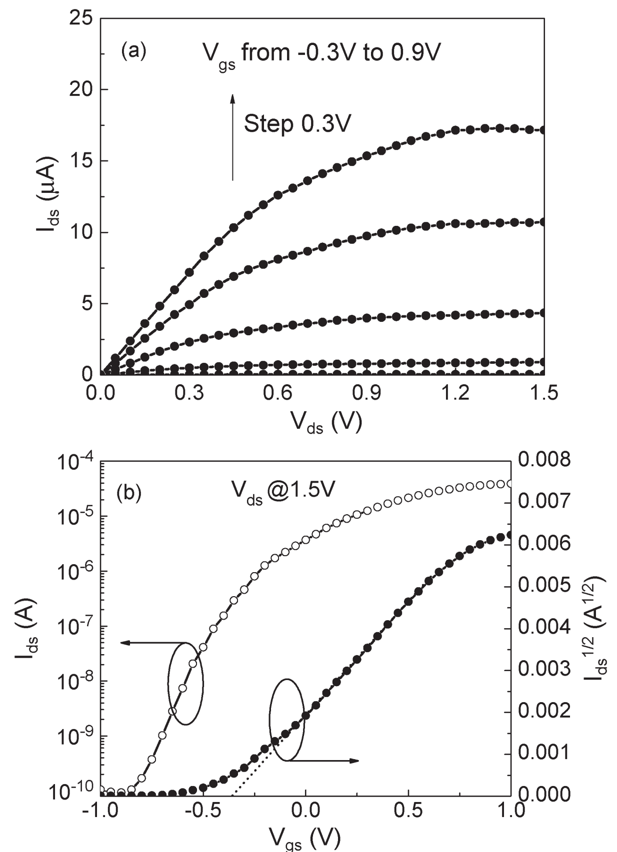

Fig. 3. (a) Output characteristics ($I_{\rm ds}$ versus $V_{\rm ds}$). (b) Transfer characteristics ($I_{\rm ds}$ versus $V_{\rm gs}$ and $I_{\rm ds}^{1/2}$ versus $V_{\rm gs}$) of the IZO-based in-plane-gate junctionless TFTs.

IZO arrays are with the dimensions of 0.5 mm × 0.2 mm. The source and the drain are obtained on the same patterned IZO film, whereas another patterned IZO film works as the gate electrode. The capacitors (C1, C2, and C3) are effectively coupled through the bottom conducting ITO films, as shown in Fig. 1(d). Both the channel width W and the channel length L is 0.2 mm. The capacitance–frequency measurement of the SiO_2-based solid electrolyte was performed using a Solartron 1260A impedance/gain-phase analyzer. The electrical characteristics of the junctionless TFTs were measured with a Keithley 4200 semiconductor characterization systems (SCS) at room temperature in the dark.

III. Results and Discussion

Fig. 2(a) illustrates the optical transmission spectra of the entire TFT arrays on the glass substrate in the wavelength range between 200 and 1000 nm. The average transmittance in the visible range (400–800 nm) is ∼75%, indicating that the TFTs are transparent to visible light. The lower middle inset shows the top-view optical image of the IZO-based in-plane-gate junctionless TFTs in electrical measurement. The lower right inset shows the image of the laser-pattered in-plane-gate junctionless TFT arrays on a glass substrate. We can see through the chip of the Logo of Chinese Academy of Sciences, indicating its transparent nature. Fig. 2(b) shows the specific gate capacitance and the ionic admittance of the SiO_2-based solid electrolyte from 0.1 Hz to 1.0 MHz using an IZO/SiO_2 electrolyte/ITO in-plane test structure. The capacitance increases with decreasing frequency, whereas the ion admittance decreases with the decreasing frequency. A maximum capacitance of 4.0 μF/cm^2 is obtained at 0.1 Hz due to the formation of the electric double layer (EDL) at the electrolyte/IZO interface. A low leakage current of below 3 nA was measured for the same in-plane test structure (not shown here), which guarantees that the transistor performance would not be affected by the leakage [5]. The results here strongly indicate that the room-temperature-deposited SiO_2 nanogranular film is not only an electronically insulating solid electrolyte but also a proton-conducting solid electrolyte [8], [9] and is desirable for low-voltage operation of junctionless oxide-based TFTs [5].

Fig. 3(a) shows the output characteristics ($I_{\rm ds}$ versus $V_{\rm ds}$ curves) at $V_{\rm gs}$ varied from -0.3 to 0.9 V in 0.3-V steps. A maximum ON-current of ∼17.5 μA was measured at $V_{\rm ds} = 1.5$ V and $V_{\rm gs} = 0.9$ V. The device shows good current saturation at high $V_{\rm ds}$ and good linear characteristics at low $V_{\rm ds}$, indicating a low resistance of the ohmic contact. Fig. 3(b) shows the transfer characteristics ($I_{\rm ds}$ versus $V_{\rm gs}$), which were measured by the sweeping $V_{\rm gs}$ from -1.0 to 1.0 V with a constant $V_{\rm ds}$ of 1.5 V. The subthreshold swing S, the threshold voltage $V_{\rm th}$, and the ON/OFF current ratio $I_{\rm on}/I_{\rm off}$ are estimated to be ∼0.12 V/dec,

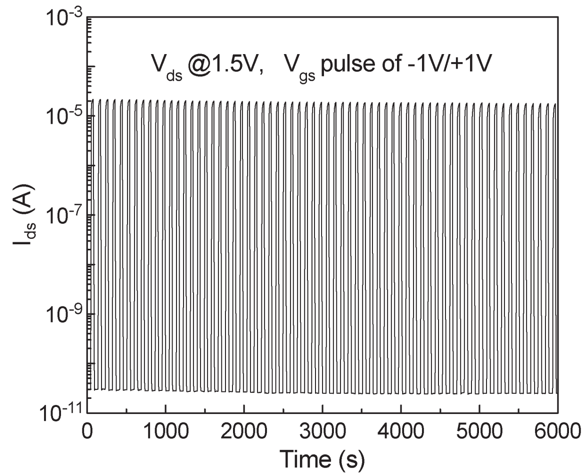

Fig. 4. Transient response of the laser-patterned IZO-based in-plane-gate junctionless TFTs to square-wave pulses of $V_{\rm gs} = -1.0$ V/1.0 V and $V_{\rm ds} = 1.5$ V.

-0.4 V, and $\sim 4 \times 10^5$, respectively. The field-effect mobility μ in the saturation region can be extracted from the relationship as follows:

$$I_{\rm ds} = \left(\frac{WC_i\mu}{2L}\right)(V_{\rm gs} - V_{\rm th})^2, \qquad (V_{\rm ds} > V_{\rm gs} - V_{\rm th})$$

where $L = 0.2$ mm is the channel length, $W = 0.2$ mm is the channel width, and $C_i = 4.0\ \mu$F/cm^2 is the specific gate capacitance of the SiO_2 electrolyte film. The field-effect electron mobility is estimated to be $\sim$15 cm^2/V $\cdot$ s.

Fig. 4 illustrates the pulse response of $I_{\rm ds}$ at a constant $V_{\rm ds}$ of 1.5 V under a square-shaped $V_{\rm gs}$ with a pulsed amplitude of -1.0 V and 1.0 V. The junctionless TFT exhibits a reasonable reproducibility of the current response to the repeatedly pulsed $V_{\rm gs}$. No ON-current loss and a maintainable $I_{\rm on}/I_{\rm off}$ ($\sim 10^5$) are obtained in response to the repeatedly pulsed $V_{\rm gs}$ ($\sim$60 testing cycles). It was reported that the $I_{\rm ds}$ value would not return to its original value after gate scanning when there is chemical doping or a chemical reaction at the interface [10]. Our results suggest that no chemical reaction is expected at the SiO_2 electrolyte/IZO interface when the gate is biased.

Finally, logic operations of the TFTs in a dual in-plane-gate configuration are also studied. Fig. 5 illustrates the logic performance. High state ("1") at 1.5 V or low state ("0") at -1.5 V are directly and independently inputted to each of the two gates (G1 and G2) as input 1 and input 2, respectively. The drain currents are detected as output ("1": $I_{\rm ds}$ above 10 μA; or "0": $I_{\rm ds}$ below 0.1 nA). When a low signal is applied to either gate of input 1 or input 2, the IZO channel is effectively modulated to a depletion region, and the high signal to another input cannot accumulate the IZO channel effectively; therefore, only a low current (< 0.1 nA) is detected. While a high signal is applied to each gate (input 1 and input 2), the IZO channel works in an accumulated region with a high current ($> 10\ \mu$A). The results indicate an AND logic with a high ON/OFF ratio of $> 10^5$ between the two logic states.

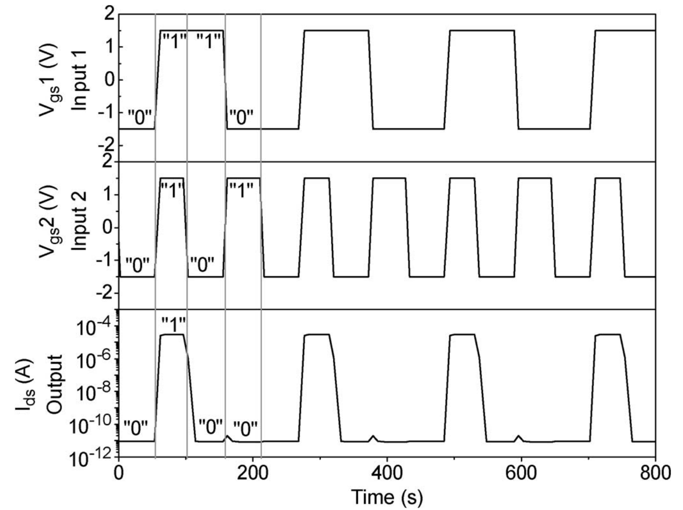

Fig. 5. AND logic operation of the IZO-based in-plane-gate junctionless TFTs with a dual in-plane-gate configuration.

IV. Conclusion

In summary, a laser-scribing process without any mask or photolithography is developed for transparent in-plane-gate junctionless oxide-based TFT array fabrication at room temperature. Such junctionless TFTs feature that the channel and the source/drain electrodes are of the same IZO film. Good electrical performance with an $I_{\rm on}/I_{\rm off}$ ratio of 4×10^5, a field-effect mobility of 15 cm^2/V $\cdot$ s, and a subthreshold swing of 0.12 V/dec is obtained. AND logic is realized with a reliable logic operation in a dual in-plane-gate configuration. The developed laser-scribing technology is highly desirable in terms of the low-cost fabrication process.

References

[1] C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J. P. Colinge, "Junctionless multigate field-effect transistor," *Appl. Phys. Lett.*, vol. 94, no. 5, pp. 053511-1–053511-3, Feb. 2009.

[2] J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. ONeill, A. Blake, M. White, A. M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," *Nat. Nanotechnol.*, vol. 5, no. 3, pp. 225–229, Feb. 2010.

[3] C.-J. Su, T.-I. Tsai, Y.-L. Liou, Z.-M. Lin, H.-C. Lin, and T.-S. Chao, "Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels," *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 521–523, Apr. 2011.

[4] J. Jiang, J. Sun, W. Dou, B. Zhou, and Q. Wan, "Junctionless in-plane-gate transparent thin-film transistors," *Appl. Phys. Lett.*, vol. 99, no. 19, pp. 193502-1–193502-3, Nov. 2011.

[5] J. Jiang, J. Sun, W. Dou, and Q. Wan, "Junctionless flexible oxide-based thin-film transistors on paper substrates," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 65–67, Jan. 2012.

[6] H. Shin, B. Sim, and M. Lee, "Laser-driven high-resolution patterning of indiumtin oxide thin film for electronic device," *Opt. Lasers Eng.*, vol. 48, no. 7/8, pp. 816–820, Jul./Aug. 2010.

[7] H. Lee, H. Shin, Y. Jeong, J. Moon, and M. Lee, "Laser-direct photoetching of metal thin film for the electrode of transistor," *Appl. Phys. Lett.*, vol. 95, no. 7, pp. 071104-1–071104-3, Aug. 2009.

[8] V. G. Ponomareva, G. V. Lavrova, and L. G. Simonova, "Effect of SiO_2 morphology and pores size on the proton nanocomposite electrolytes properties," *Solid State Ionics*, vol. 119, no. 1–4, pp. 295–299, Apr. 1999.

[9] M. Nogami, R. Nagao, C. Wong, T. Kasuga, and T. Hayakawa, "High proton conductivity in porous P_2O_5–SiO_2 glasses," *J. Phys. Chem. B.*, vol. 103, no. 44, pp. 9468–9472, Oct. 1999.

[10] H. Yuan, H. Shimotani, A. Tsukazaki, A. Ohtomo, M. Kawasaki, and Y. Iwasa, "High-density carrier accumulation in ZnO field-effect transistors gated by electric double layers of ionic liquids," *Adv. Funct. Mater.*, vol. 19, no. 7, pp. 1046–1053, Apr. 2009.